RELIABILITY, POWER DISSIPATION, SENSING, AND THERMAL TRANSPORT IN CARBON NANOMATERIALS AND DEVICES

BY

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DISSERTATION

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ABSTRACT

Energy consumption is a significant challenge across the globe ranging from power consumption in large-scale buildings to nanoscale devices. A fundamental examination of energy dissipation in such contexts can lead to orders of magnitude improvements in energy efficiency. Emerging classes of nanomaterials, such as carbon nanotubes and 2-dimensional crystals (e.g. graphene), have presented new opportunities to improve energy use at the macro and nanoscale. However, much work remains to be done to fully understand the high-field reliability and fundamental properties of these nanomaterials in order to promote their widespread use in energy applications.

In this work, we investigate the reliability of carbon nanotube transistors by developing a pulsed measurement technique to suppress hysteresis for carbon nanotube (CNT) mobility measurements in air, in vacuum, and over a wide (80 – 453 K) temperature range. The use of this pulsed measurement technique provides a route towards measuring the device mobility without the effects of charge screening as well as the interface quality of low-dimensional systems and their surrounding bulk environments. We then use infrared thermometry to investigate power dissipation in carbon nanotube network (CNN) transistors and find the formation of distinct hot spots during operation. However, the *average* CNN temperature at breakdown is significantly lower than expected from the breakdown of individual nanotubes, which we attribute to extremely high regions of power dissipation at the nanotube junctions.

We then turn our attention to the fundamental properties of large-scale polycrystalline graphene films grown by chemical vapor deposition (CVD). We elucidate the chemical sensing mechanisms of such films, and find that linear defects or continuous lines of point defects are needed to enhance the chemical sensitivity of graphene. Therefore, simple chemiresistors made

from CVD polycrystalline graphene could be used as highly sensitive pollutant detectors in "smart" climate control systems to reduce energy consumption by residential and commercial buildings. Lastly, we develop an electrical thermometry platform to investigate the practical tuning of thermal transport in layer-by-layer assembled graphene van der Waals (vdW) solids. We find thermal transport in a single layer of transferred CVD graphene is limited by substrate phonon and grain boundary scattering, but can be significantly enhanced by transferring subsequent layers of CVD graphene.

Overall, the research summarized in this dissertation represents a significant advancement in the understanding of the reliability and fundamental physical properties of emerging nanomaterials, which are increasingly finding their way to commercial applications.

To Isaac Marshall Estrada

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CHAPTER 1

INTRODUCTION

1.1 Energy Consumption in the United States

Some of the greatest scientific and engineering challenges for the 21st century involve developing widely distributed renewable energy systems while reducing energy consumption and mitigating CO_2 emissions from the combustion of fossil fuels. A quick review of global energy consumption reveals the enormity of these challenges. Data collected by the International Energy Agency indicate global energy consumption has doubled over the past 30 years, reaching 8.7 million tons of oil equivalent (Mtoe) in 2010 [1]. Moreover, ≈66% of the world's energy is produced from the combustion of fossil fuels (e.g. oil, coal, and natural gas) which account for 99.6% (≈30.3 Gt) of energy production related CO_2 emissions [1]. Increasing energy demand is driven in large part by technological advances in underdeveloped countries, i.e. those that are not members of the Organization for Economic Cooperation and Development (OECD). In 2010, non-OECD countries consumed ≈55% of the global energy produced while OECD member countries consumed the remainder (Figure 1.1) [2]. This share is slowly increasing as non-OECD members improve their power infrastructures and gain increased access to advanced information

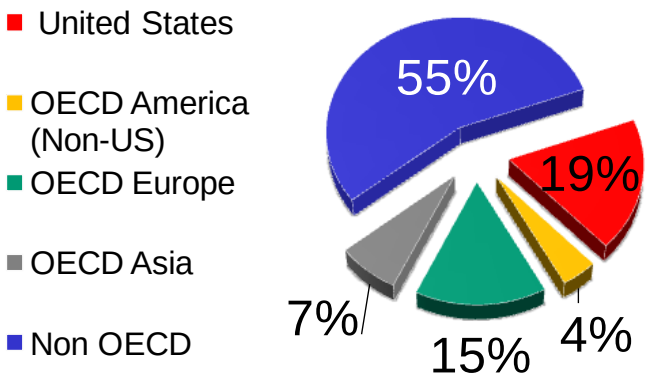

Figure 1.1 Percentage of global energy consumed in 2010 by OECD and non-OECD members. The United States consumed almost 1/5 of the global energy produced.

and computing technologies.

Such grand challenges, however, often present great opportunities. For example, the United States consumed ≈19% of the world's energy in 2010 (Figure 1.1) [2]. It is interesting to note that the United States consumed more energy than any other OECD member, and that 80% of the energy produced within the United States was through the use of fossil fuels [2]. Furthermore, ≈50% of the energy produced in the United States is wasted before end use, largely in the form of heat [3]. Taking a closer look at energy use in the United States reveals that 41% is consumed within the residential and commercial building sectors, which includes computers and electronics [4].

Herein lay the opportunities for energy conservation, as advances in heating, ventilation, air conditioning (HVAC) systems, as well as low-power nanoelectronics are poised to make a global impact on energy use. In the United States, computers, electronics, and HVAC systems account for over 50% of energy end use in the building sector (Figure 1.2) [4]. Most HVAC systems refresh the air inside a building by continuously ventilating with outside air. This air must be heated or cooled to match the temperature set point of the building's climate control

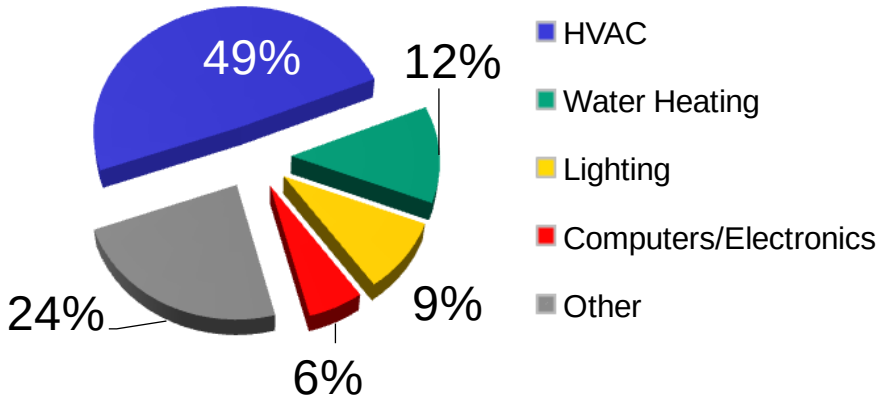

Figure 1.2 Percentage of energy consumed within the United States building sector by end use. Computers, electronics, and HVAC systems account for over 50% of energy consumed by the United States building sector.

system, resulting in wasted energy. Advanced pollution and CO_2 sensors could be coupled with sophisticated feedback systems to develop "smart" HVAC systems. Such systems could monitor air quality and refresh air only in rooms which exceed specified thresholds by recycling air from unoccupied portions of the building or from outside the building when necessary.

While HVAC systems certainly consume enormous amounts of energy, computer-related energy consumption is rapidly increasing and poses a significant challenge in meeting the energy demands of the growing information and computing technology infrastructure. The typical PC and server waste more than 30% of their input power in the form of heat. This wasted energy has yet to be harnessed to perform work, such as switching transistors or storing data in a memory bit. To compound the problem, the amount of waste heat generated requires advanced thermal management techniques, and increases demands on auxiliary systems such as air conditioning, which results in higher energy requirements and cost [6]. Figure 1.3 (A) illustrates the breakdown of computer-related energy use reported in the United States for the year 2007 in gigawatts. When cooling is added to the energy use of data centers, PCs, and displays, computer-related energy consumption accounts for 5% of the nation-wide power budget in 2007

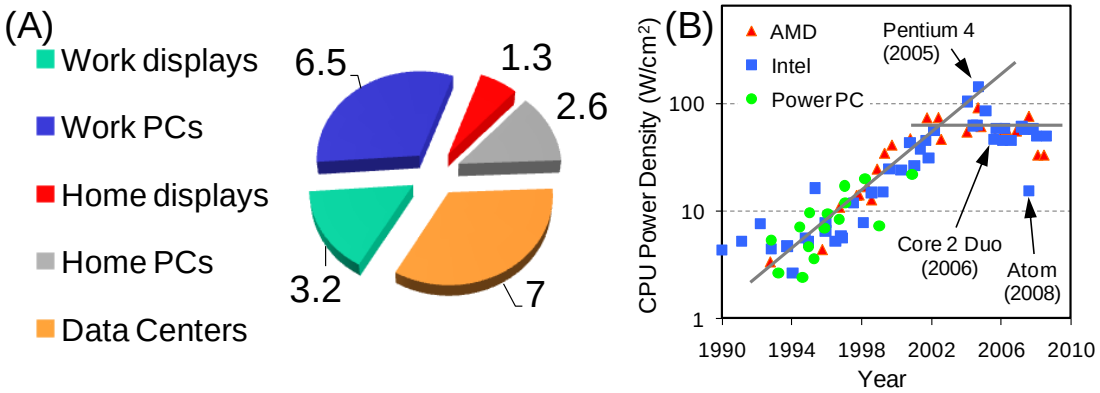

Figure 1. 3 (A) Total U.S. computer-related power consumption in 2007 separated by computer sector for 2007 in gigawatts. In 2007 computer-related energy use accounted for 5% of the national power budget. **(B)** Power density vs. time for major computer processors manufactured over the past two decades. The exponential trend in power density has limited transistor scaling and is the main source for computer-related energy consumption. Figures reproduced from [5].

[5]. If current trends continue, it is expected that computer-related energy use would require 1/3 of the national power budget in the year 2025 [5, 7].

One of the major influences on the increased power dissipation in computers is an exponential increase in the power density of computer processors (Figure 1.3 (B)). Current computer processor technology has a power density of about 100 W-cm^{-2}, approximately equal to that of an incandescent light bulb. Power density in integrated circuits is a result of leakage currents (I_{LEAK}) in transistors, $P_{STATIC} = I_{LEAK} * V_{DD}$, and increased dynamic power consumption, $P_{DYN} = f * C * V_{DD}^2$. Here, f is the clock frequency, C is the load capacitance, and V_{DD} is the operating voltage [5]. While transistor scaling has lowered the required operating voltages, faster switching speeds and increased leakage currents continue to dominate the resultant power densities. Hence, commercial nanoelectronics technology is limited by power dissipation, affecting performance from mobile devices to large data centers [5].

1.2 Carbon Nanotubes and Graphene

Among possible candidates for developing highly sensitive gas detectors and replacing silicon in nanoelectronics are sp^2 hybridized carbon nanomaterials, e.g. 1-dimensional (1D) single-wall carbon nanotubes (SWCNTs) and 2-dimensional (2D) graphene (Figure 1.4). Graphene is an atomic monolayer of carbon atoms arranged in a honeycomb lattice [8]. SWCNTs can be visualized as graphene "rolled up" into a cylindrical nanostructure [9]. These materials not only offer a high specific surface area [10-11], but they exhibit excellent thermal [12-13] and electrical conductivities [8, 14], which benefit from strong sigma bonds, symmetric energy bands for electrons and holes (Figures 1.4 (C) and (D)), and high optical phonon energies (~180 meV). These physical properties have prompted their use as circuit elements, e.g.

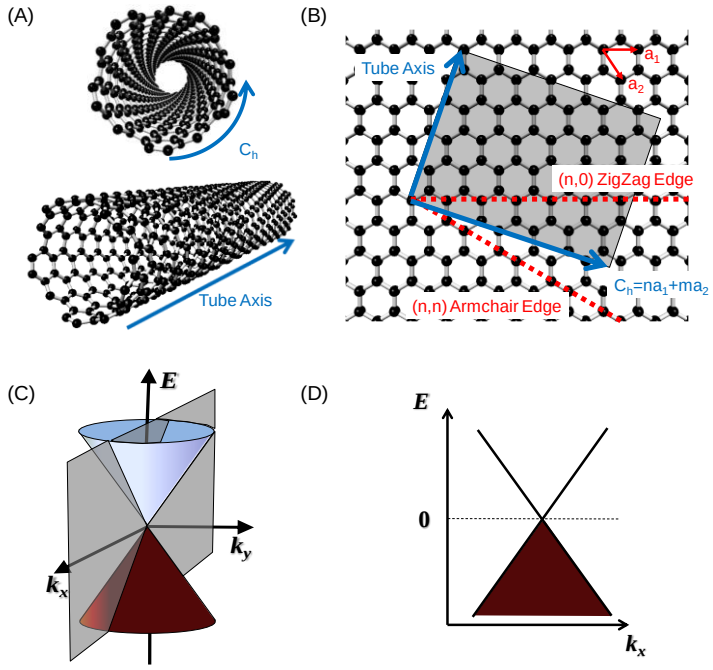

Figure 1. 4 (A) SWCNT showing the chiral (C_h) and tube axis vectors. **(B)** Graphene sheet illustrating how SWCNTs can be "rolled up" from graphene with (n, m) chiral indices. The graphene unit vectors (a_1 and a_2) are also shown. **(C)** Energy vs. momentum dispersion relationship of graphene near the K point of the Brillion Zone. **(D)** 2-dimensional cross section of the graphene dispersion in (C) illustrating how the energy dispersion of CNTs can be simply related to that of graphene. In this particular case, the cross section is taken at the Dirac point (where the conduction and valence bands touch) resulting in a linear band structure without a band gap, i.e. a metallic SWCNT. A full treatment of the tight-binding formalism for graphene and SWCNTs can be found in [20].

transistors [8, 15] and interconnects [16-17]. They have also been investigated as thermal heat sink components [18] and thermal interface materials [19].

Because of the high electric field or temperature gradients associated with these applications, it is important to fully characterize their fundamental properties and their reliability under such stress. Therefore, developing future nanocarbon technologies requires (1) innovations in integration of carbon into novel nanomaterials systems, (2) advances in nanomaterials synthesis methods which are compatible with existing planar processing technologies, and (3) an increased fundamental understanding of the physical properties of these materials and how those properties are affected by external influences and defects.

1.3 Organization of Dissertation

In this study, we investigate various aspects of reliability, power dissipation, chemical sensing, and thermal transport in carbon nanomaterials and devices. This work is largely experimental and supported with simulations mainly done with the help of our collaborators.

In Chapter 2, we review fundamental concepts of thermal transport in semiconductors, metals, and across interfaces. We also discuss size effects on thermal transport by reviewing thermal transport from bulk silicon and germanium to their nanoscale counterparts. Similarly, we illustrate the role of substrates, carbon nanotube (CNT) – CNT junctions, and graphene nanoribbon edges on thermal transport in carbon nanomaterials.

In Chapter 3, a pulsed technique to suppress hysteresis in CNT transistor transfer characteristics is demonstrated. As hysteresis is reduced, both forward and backward gate voltage sweeps move towards a common, unique central transfer characteristic which reveals the "true" device mobility. The developed technique offers a useful metrology method to reliably extract device parameters without the effects of charge screening.

In Chapter 4, we use infrared (IR) microscopy to investigate power dissipation in CNT network thin-film transistors. We find that the average temperature rise imaged by IR microscopy near device failure is much lower than the oxidation temperature of individual CNTs in air. Using this information, we develop a thermal model which highlights the role of crossed CNT junctions in limiting the thermal reliability of our devices.

In Chapter 5, we study the chemical sensing properties of graphene grown by chemical vapor deposition (CVD) in a simple chemiresistor structure. These films are found to be more sensitive to target analytes than previously developed CNT chemiresistors. The chemical sensitivity is further enhanced when the graphene is patterned into microribbon structures. We

attribute the chemical sensitivity of CVD graphene to the defective nature of the CVD graphene film.

In Chapter 6, we present the design of an electrical thermometry platform for measuring the thermal properties of nanoscale films. We use this platform to measure the thermal properties of millimeter-scale CVD graphene films and correlate their thermal properties to substrate and grain boundary scattering. Furthermore, we show how the thermal conductivity of CVD graphene films can be increased through layer-by-layer assembly of graphitic thin films.

Finally, in Chapter 7, we summarize the key findings and conclusions of this body of work, and give recommendations for possible future study.

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CHAPTER 2

FUNDAMENTALS OF THERMAL TRANSPORT IN EMERGING NANOMATERIALS

One of the most difficult challenges facing the semiconductor industry is the development and/or discovery of novel materials to replace silicon within the transistor channel, while maintaining a relatively high carrier mobility and simultaneously reducing power dissipation [1]. Addressing this challenge will require integration of dissimilar materials of varying dimensionality. For example, compound semiconductors and germanium are candidate materials for integration with future silicon complementary metal-oxide-semiconductor (CMOS) technology beyond the 22 nm node [2]. Such channel materials will likely be integrated with high-κ dielectrics in multi-gate or wrap around gate nanowire-like field-effect transistors (FETs), i.e. FinFETs. These devices offer greater electrostatic control over the device channel and lower threshold voltages [3-4]. 1-dimensional (1D) carbon nanotubes [5] (CNTs) and 2-dimensional (2D) crystals such as graphene [6] and molybdenum disulfide (MoS_2) [6-8] have also attracted much attention from the device research community, and are firmly on the International Technology Roadmap for Semiconductors (ITRS) as emerging research devices and future CMOS technologies [2].

In all cases, the use of dissimilar materials presents more than just a materials synthesis and integration problem. The underlying challenge remains one of power dissipation in nanoscale transistors and interconnects because of unsustainable high temperatures reached during high-frequency operations. This temperature rise limits the density of devices and the operating frequency of computer processors. In its simplest form, the temperature rise in a device can be written as $\Delta T = P \times R_{TH}$, where P is the power dissipated in the device and R_{TH} is the lumped thermal resistance of its environment [9]. The thermal resistance depends on the device

geometry and thermal conductivity (κ) of the material, i.e. $R_{TH} = \frac{t}{\kappa A}$, where t is the thickness of the layer that conducts the heat and A is its cross-sectional area. From an engineering point of the view, the device geometry can be designed to facilitate heat spreading. For example, recent reports from our group have shown the current carrying capability of 1D carbon conductors benefit from 3-dimensional (3D) heat spreading into 3D substrates [10-11]. From a fundamental point of view, however, it is important to understand the role of thermal conductivity and thermal transport across interfaces in the novel materials systems being developed for future nanoelectronics applications. Therefore, this section reviews basic heat flow in semiconductors, metals (e.g. Cu), and interfaces. We also discuss size effects on thermal transport resulting from edges and boundaries, as well as dimensionality effects, by reviewing thermal transport at 0-dimensional (0D) nanotube junctions, 1D nanotubes and nanowires, and 2D graphene nanomaterials. Taking advantage of this information, new families of electronic devices could be designed, which are more energy efficient from the outset, in part alleviating heat dissipation problems before they begin.

2.1 Thermal Transport in Semiconductors, Metals, and across Interfaces

Heat flows through a medium across a temperature gradient from the hot to the cold side. It is typically described on the basis of Fourier's law, which relates the heat flux (q) to the temperature gradient (∇T) through a scalar quantity known as the thermal conductivity (κ), i.e. $q = -k\nabla T$. The κ is a materials-dependent property which varies with temperature and the dimensionality of the system. In macroscopic solids, κ has contributions from phonons (κ_p) and electrons (κ_e). In general the thermal conductivity of phonons can be written as

$$k_p = \frac{1}{d}\frac{\partial}{\partial T}\int f(E)g(E)v(E)\Lambda(E)dE \tag{2.1}$$

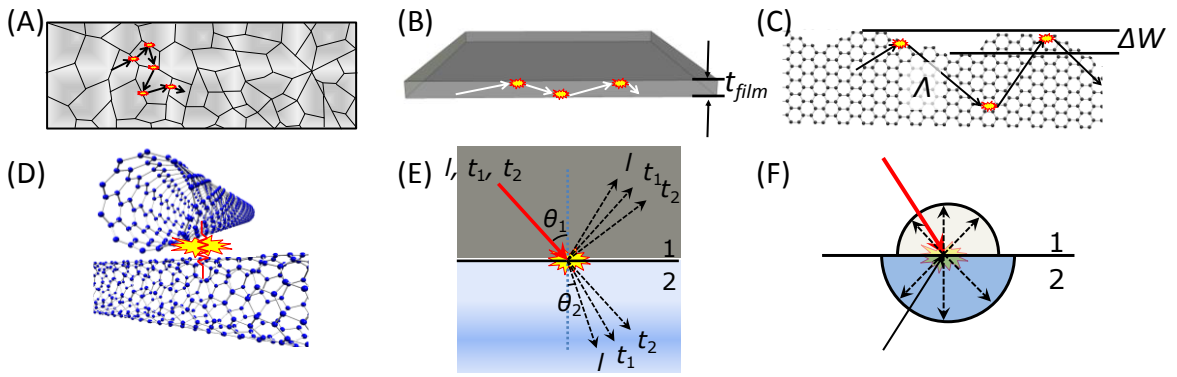

Figure 2.1 Several phonon scattering mechanisms in solids. (**A)** Grain boundary scattering where the phonon mean free path (Λ) is limited by scattering at the interfaces of adjoining grains. **(B)** Boundary scattering in a thin film where the thickness (t_{film}) is less than Λ. (**C)** Edge roughness (ΔW) scattering in a graphene nanoribbon where ΔW introduces additional scattering as compared to boundary scattering. (**D)** Interface scattering at crossed CNTs where the extremely small area for phonon transmission across the interface results in a high thermal resistance. (**E)** Acoustic mismatch model (AMM) of interface scattering where an incident phonon (red arrow) reflects or transmits (dashed arrows) depending on the angle of incidence (θ_1). **(F)** Diffuse mismatch model (DMM) where incident phonons scatter at the interface depending on the available states on both sides of the

where d is the dimensionality of the system, $f(E)$ is the probability distribution function, $g(E)$ is the density of states, $v(E)$ is the phonon group velocity, and $\Lambda(E)$ is the mean free path. It is important to note $\Lambda(E)$ is the inverse of the time between scattering events, which contains contributions from various scattering mechanisms all summed using Matthiessen's rule. Figure 2.1 illustrates several phonon scattering mechanisms which can reduce κ.

For 3D materials, the specific heat (C_p) can be related to κ_p using simple kinetic theory, as $\kappa_p \approx (1/3) \times CV\Lambda$. This approximation is valid when thermal transport is diffusive, i.e. the path for heat flow is much larger than Λ. Using this simple analysis, one can relate the thermal conductivity to the mass of the sample. The specific heat is the amount of thermal energy gained or lost by a material due to a temperature change, i.e. $C_p = Q/m \times \Delta T$. Here, Q is the heat flux and m is the mass of the sample. In addition, from a classical point of view, phonons are often compared to the oscillations of a mass and spring system, and the phonon velocity is then inversely proportional to the square root of strength of bonding between atoms (spring constant –

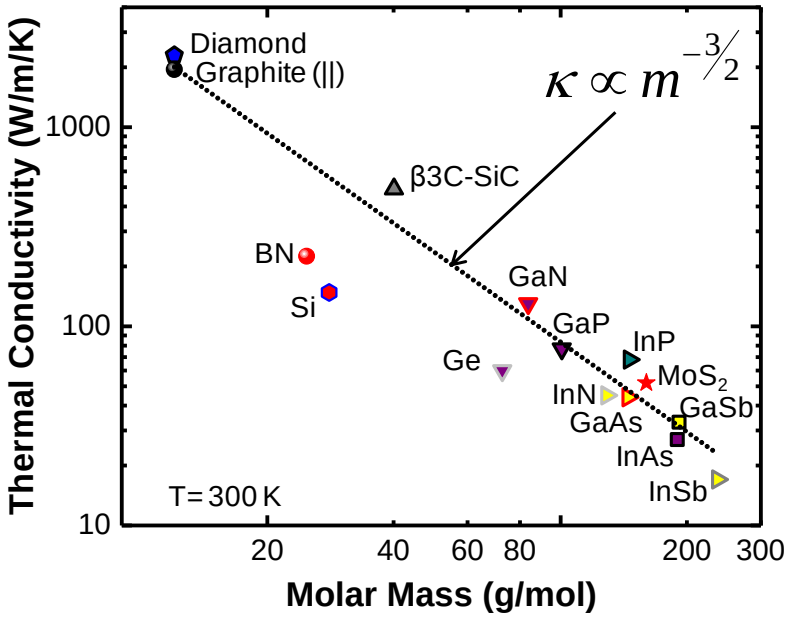

Figure 2.2 Thermal conductivity vs. molar mass for various materials and semiconductors relevant to the ITRS emerging research devices and materials roadmaps. Type 2 A diamond, pyrolytic graphite (||), Si, Ge [12], GaN – wurtztite [13], InN [14], BN [15], SiC [16], GaP, GaAs, GaSb, InAs, InSb, InP [17], and MoS_2 [18]. The dashed line shows a power law fit to $m^{-3/2}$.

k') divided by the mass of the atoms, i.e. $v \propto \sqrt{k'/m}$. If we assume Λ does not depend on the mass then we can expect κ_p will decrease with increasing mass for bulk solids, following a power law with $m^{-3/2}$. Figure 2.2 shows the thermal conductivity of various materials as a function of the molar mass. The dashed line shows the power law fit with the exponent fixed, i.e. $\kappa = a \times m^{-3/2}$ where a is a constant. The reported values for κ of the various materials show remarkably good agreement with the power law fit, providing a basic understanding of how thermal conductivity is affected by optical phonon energies and the atomic masses of the elements in a material.

In contrast to intrinsic semiconductors, the thermal conductivity of metals is dominated by a free electron gas. Therefore, for diffusive thermal transport the electronic contribution to the thermal conductivity can be approximated as

$$k_e = \frac{1}{3}\left(\frac{\pi^2}{2}k_B^2 n\frac{T}{E_F}\right)v_F l = \frac{1}{3}C_e v_F \Lambda \tag{2.2}$$

where k_B is the Boltzman constant, E_F is the Fermi level, v_F is the electron Fermi velocity, C_e is the electron volumetric specific heat. At low temperatures, $C_e \propto T$, while at higher temperatures (~ ½ Debye temperature (Θ_D)) $\Lambda \propto \frac{1}{T}$. The Debye temperature is a typical figure of merit for the temperature at which a material's molar specific heat capacity obeys the Dulong-Petit law. Therefore, inspection of Equation 2.2 shows κ_e can become independent of temperature when the temperature dependence of these two effects balances. This is discussed in more detail in a recent review by Toberer et al. [19].

Because the electrons in a metal conduct charge as well as heat, the electrical conductivity of metals (σ) can be related to κ through the Weideman-Franz law, i.e. $L = \frac{\kappa}{\sigma T}$.

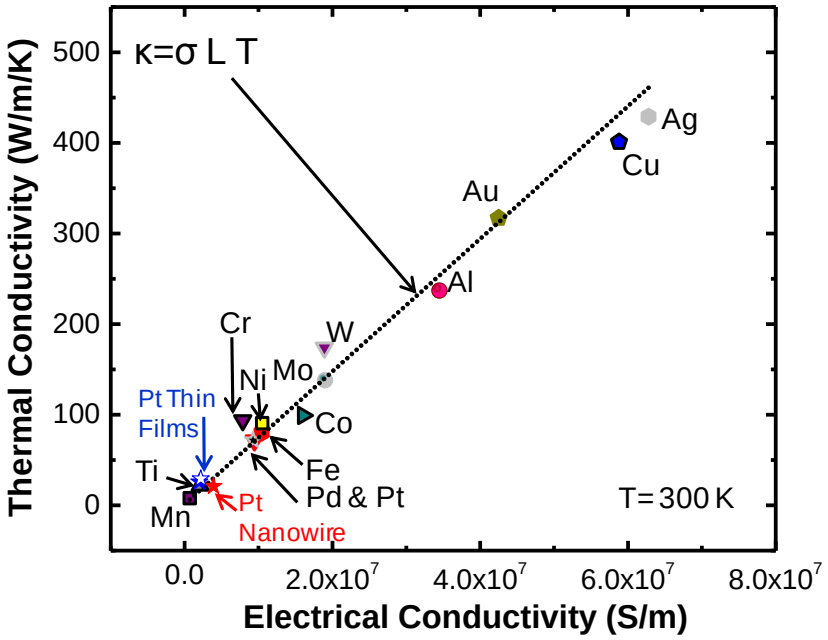

Figure 2.3 Thermal conductivity vs. electrical conductivity for various metals. Thermal conductivity of bulk metals: Al, Cr, Co, Cu, Au, Fe, Mn, Mo, Ni, Pd, Pt, Ag, Ti, W [12]. The electrical conductivity of bulk metals: Al, Cu, Au, Fe, Mo, Ni, Pt, Ag, Ti, W, Cr, Co, Mn, Pd [20]. Data from the Pt nanowire is from [21]. Data for the Pt thin films are from [22-23].

Here, L is the Lorentz number, which is defined as $L = \frac{\pi^2}{3}\left(\frac{k_B}{e}\right)^2 = 2.45\times10^{-8}\left(W\,\Omega\,K^{-2}\right)$, and where e is the elementary charge. Figure 2.3 illustrates the Weideman-Franz law for various metals. It is readily seen that bulk metals with high σ also have high κ_e (e.g. Ag and Cu), while those with low σ also exhibit low κ_e (e.g. Ti and Mn). Numerous studies have investigated confinement effects on the σ and κ of metal thin films and nanowires [21-25]. In all cases, the nanoscale metal films and wires show a significant reduction in the σ/κ ratio. These reductions are attributed to increased effects of grain and boundary scattering on the electrical and thermal transport. For example, Zhang et al., found that the σ and κ for 28 nm thick Pt films were reduced to approximately 23% and 41% of their corresponding bulk values [23], respectively. The calculated Lorentz number for these nanoscale thin films would then be ~$4.5\times10^{-8}\ W\,\Omega\,K^{-2}$, a significant deviation from the Weideman-Franz law for bulk Pt. The observed reduction in σ and κ in nanoscale metal films has significant implications for metal interconnects in future CMOS technologies, because line widths and film thicknesses are expected to decrease further into this nanoscale regime in order to accommodate shrinking devices and more complex circuits in 3D architectures. Lower σ and κ in nanoscale metal interconnects will result in increased power dissipation and longer signal delays. The semiconductor industry is working diligently to solve the complex issues surrounding interconnects, including investigating the possibility of replacing metal interconnects with novel materials such as graphene and carbon nanotubes [1].

The performance of future nanoscale electronics is expected to benefit from replacing silicon with materials which have better intrinsic properties. For example, carbon nanotubes which exhibit higher carrier mobility (μ) and κ than silicon are already finding their way into various commercial electronics applications, particularly where they outperform amorphous silicon [26]. Although the individual device performance may benefit from new materials, power

dissipation and energy transport in a system composed of nanoscale elements is still likely to be limited by interfaces. This limitation is attributed to the thermal boundary resistance (Kapitza resistance) which exists at the interfaces of dissimilar materials. The inverse of the Kapitza resistance is referred to as the thermal boundary conductance (G). When a heat flux (q) flows across a boundary, it results in a temperature drop (ΔT) at the interface, which is characterized by G, i.e. $q = G\Delta T$. The first measurements of this phenomena were reported by Kapitza who measured the temperature drop across the interface between helium and various metals [27]. More recently, experimental techniques such as the 3-omega method and the time domain thermoreflectance (TDTR) have been developed to investigate g of various materials systems [28-31]. A recent review by Pop summarizes key experimental findings for thermal transport across interfaces between bulk solids [9]. The experimental data are found to approach two limits, with the best interfaces for thermal transport being between metals with high σ (e.g. Al/Cu) where electrons carry the heat across the interface [32]. The worst interfaces are those where phonons carry the heat across the interface of materials, with a large mismatch in Θ_D, e.g. Bi/H-diamond [33].

Thermal transport across interfaces is typically modeled by either the acoustic mismatch model (AMM) [34] or the diffuse mismatch model (DMM) [35] (Figure 2.1 (E, F)). Both models consider only phonon transport across the interface, neglecting contributions from electrons. The AMM considers the wavelength and direction of the incoming phonon and assumes a perfect interface. Phonon transmission across the interface is assumed to be specular and elastic. That is, transmission across the interface is based solely on the angle of incidence and the phonon energy. An incoming phonon can reflect, transmit, and/or change polarization, but the frequency must remain the same. Experimental data usually agrees well with the AMM at low

temperatures, but does not agree well at higher temperatures where the phonon wavelengths are on the order of surface roughness at the interface. The DMM is generally used to model experimental data at high temperatures. The DMM assumes an incoming phonon can be reflected or transmitted based on the available states in each material on either side of the interface. Phonons emerging from the interface are not bound to the properties of the incident phonon, i.e. each incoming phonon loses memory of which material it originated from, and scattering at the interface is diffuse so long as there is an available state. In the DMM, phonon transmission across the interface is limited by the mismatch in the phonon density of states. It should be noted the DMM is limited in that it does not apply when the two materials on either side of the interface have similar phonon density of states. In this scenario, phonon transmission across the interface should approach 100%. However, the DMM wrongly predicts 50% transmission. The DMM is best used to model phonon transmission between highly dissimilar materials at high temperatures.

Typically, the interface between 1D or 2D nanostructures, amongst themselves or with 3D substrates, are weak contacts dominated by van der Waals (vdW) forces [36-37]. Recent reports suggest manipulating the interfacial bond strength at material interfaces improves their thermal conductance [38-40]. Hsieh et al. demonstrated the pressure tunability of weak vdW interfaces of Al/graphene/SiC. They increased *G* by approximately an order of magnitude at pressures of 10 GPa [38]. Hopkins et al. show *G* increases by a factor of two for oxygen functionalized graphene (o-graphene) at Al/o-graphene/SiO_2 interfaces as compared to unfunctionalized Al/graphene/SiO_2 interfaces [39]. Additionally, O'Brien et al. demonstrate a 4× increase in the *G* of the Cu/SiO_2 interface through chemical functionalization of the interface with strongly bonding organic nanomolecular monolayers (NMLs) [40]. Relating the effect of

the NML to the equivalent thermal impedance of a dielectric layer with thickness t and thermal conductivity κ, i.e. $G = \kappa / t$, suggests using a NML to increase the bond strength is equivalent to removing $\approx$13 nm of SiO_2 ($\kappa_{SiO_2} = 1.4$ $Wm^{-1}K^{-1}$) [9]. This result is a particularly interesting discovery as it has significant implications for current Cu interconnect technologies.

2.2 Thermal Transport in Semiconductor and Carbon Nanomaterials

Over the past few decades, the advances in synthesis, processing, and metrology of nanostructured materials have resulted in a greater fundamental understanding of nanoscale thermal transport in low-dimensional systems. In particular, the discovery and isolation of CNTs [41] and graphene [42], coupled with advanced thermometry techniques [43-45], has enabled the first experimental investigations of nanoscale thermal transport in 1D and 2D crystals. Furthermore, the use of microfabricated suspended thermometry platforms to measure thermal and thermoelectric properties of semiconductor nanowires has led to new insight into the differences in the transport properties of "bottom-up" [46] vs. "top-down" fabricated nanowires [47-48]. The latter of which could benefit from the large industrial infrastructure of top-down silicon manufacturing processing technology to produce a new class of "nanoengineered" thermoelectrics based on roughened semiconductor nanowires [48].

2.2.1 Semiconductor Nanomaterials

Figure 2.4 summarizes reported values of κ for bulk to nanostructured silicon and germanium. A quick examination of the data shows that the κ for these semiconductor materials spans 3 orders of magnitude and depends largely on temperature and the dimensions of material. For example, the bulk κ of silicon and germanium peak near 5600 and 1800 $Wm^{-1}K^{-1}$ near 25 and 10 K, respectively. Below these temperatures, κ follows the T^3 dependence of C_v; and above these temperatures, κ is dominated by phonon scattering. Also noteworthy is the doping and size

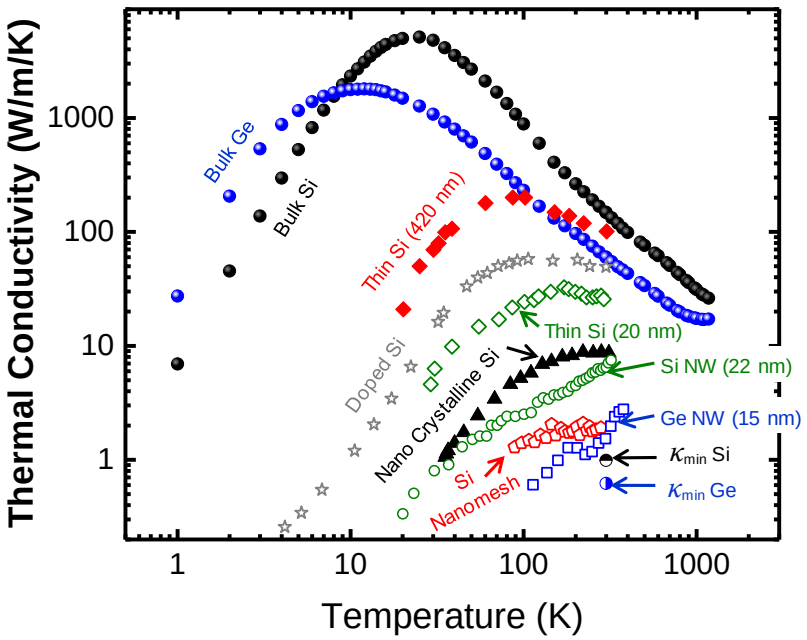

Figure 2.4 Thermal conductivity (κ) as a function of temperature: representative data for thin films of Si (420 nm – filled red diamonds [49], 20 nm – open green diamonds [50]), highly doped Si (3×10^{20} cm^{-3} of boron doping – open grey stars) [16], nanocrystalline Si (filled black triangles) [51], Si nanowire (d = 22 nm – open green circles) [46], Si nanomesh (open red pentagons) [52], Ge nanowire (d = 15 nm – open blue squares) [53], bulk Si (black spheres) [12], bulk Ge (blue spheres) [12], and minimum thermal conductivities for amorphous Si and Ge (half filled circles (up – Si) and (right-Ge), respectively) [54].

effects on the κ of semiconductor thin films, nanowires, and nanostructured materials. Slack performed some of the earliest measurements to elucidate the role of doping on the κ of silicon [16]. Highly doped silicon resulted in higher phonon-impurity scattering, and while the effects on κ are more severe at low temperatures, the room temperature κ of highly doped (3×10^{20} cm^{-3} of boron doping) silicon was reduced by a factor of 3 (reduced from 148 to 50 $Wm^{-1}K^{-1}$). The effects of boundary scattering in silicon thin films have been largely reported, and are well explained by measurements performed by Ashegi et al. They measured varying thicknesses of pure single crystal silicon on insulator films and show the room temperature κ of silicon is gradually reduced from its bulk value of 148 $Wm^{-1}K^{-1}$ down to 22 $Wm^{-1}K^{-1}$ when the film is reduced to a thickness of 20 nm. These reported values are for the κ measured parallel to the thin film boundaries. The reduction of κ is attributed to increased phonon-boundary scattering and

can be taken into account by including the appropriate scattering rate into the thermal conductivity equation [49-50].

Even greater reductions in the κ of silicon and germanium semiconductor nanowires grown by a vapor-liquid-solid (VLS) method [55] have been observed due to a further increase in phonon-boundary scattering resulting from the circular cross section of the nanowire and confinement of the acoustic phonons [46, 53]. Li et al. show the room temperature κ of VLS grown silicon nanowires with a diameter of 22 nm is reduced to about 6.5 $Wm^{-1}K^{-1}$, corresponding to $\approx$4% of the bulk silicon value [46]. Wingert et al. show a similar decrease in the room temperature κ in a germanium nanowire with a diameter of 15 nm, where the κ is reduced to about $\approx$ 3% of the bulk germanium value [53]. In both cases, the κ of semiconductor nanowires with diameter of $\approx$20 nm or below begins to approach the minimum κ (κ_{min}) limit of corresponding amorphous material [54].

The extreme reduction of κ in semiconductor nanowires is particularly interesting for two reasons. First, the 22 nm technology node for semiconductor processors has incorporated a tri-gate architecture for the transistor where the device channel is similar to a top-down defined semiconductor nanowire [4]. Therefore, the reduction in κ may have serious implications for power dissipation in future tri-gate semiconductor devices. Moreover, top-down fabrication processes are expected to add surface roughness to semiconductor nanowires, resulting in a further decrease in κ as compared to VLS grown semiconductor nanowires [47-48, 56]. Second, the extreme reduction in κ in semiconductor nanomaterials may prove beneficial for semiconductor nanomaterial based thermoelectrics [47-48].

The figure of merit (ZT) for a thermoelectric is defined as $ZT = \frac{S^2\sigma}{\kappa}$, where S is the Seebeck coefficient. If S and σ can be preserved near their bulk values, or enhanced through doping, then semiconductor nanomaterials may find widespread applications in solid-state energy conversion. In this regard, two forms of semiconductor nanomaterials show great promise. Recent work by Yu et al. shows the σ and κ of silicon phononic nanomesh structures can be independently controlled if the periodicity of the nanomesh is on the order of the phonon Λ [52]. They show an $\approx$25× reduction in κ as compared to highly doped bulk silicon, while preserving the high electrical conductivity of the nanomesh (on the order of bulk silicon) with $\approx$0.5 to 2 × 10^{19} cm^{-3} doping. Nanocrystalline semiconductor materials are also promising as they provide a low-cost alternative to nanomesh structures for possible applications in solid-state thermoelectrics. Wang et al. recently provided new insight into the effects of grain boundary scattering and porosity on thermal transport in nanocrystalline silicon [51], which could prove beneficial for designing solid-state thermoelectrics if the electronic power factor can be preserved as in other nanocrystalline films [57-59].

2.2.2 Carbon Nanomaterials

Several recent reviews provide an in-depth analysis of thermal transport in carbon nanomaterials [60-62]. Therefore, in this section we focus on the role of the substrate and edges on thermal transport in substrate supported graphene and graphene nanoribbons. We also review thermal transport in bulk-like carbon nanotube films, highlighting the role of 0D crossed nanotube junctions on tuning the thermal transport of CNTs from thermal conductors to thermal insulators. The intrinsic in-plane thermal conductivity ($\kappa_{||}$) of these materials is the highest of any known material ever measured [45, 63-64], which makes them ideal systems to investigate

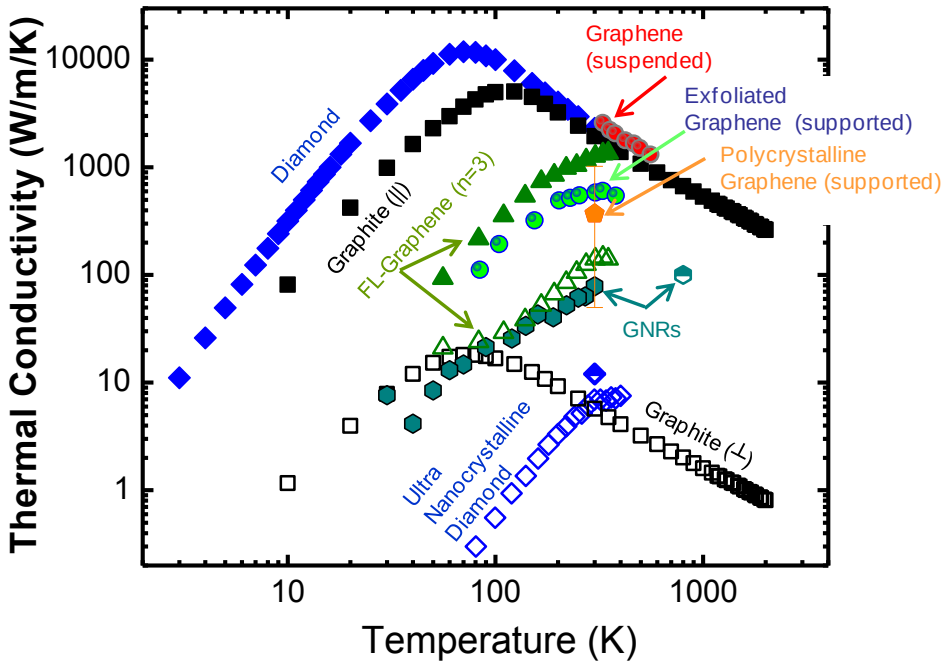

Figure 2.5 Thermal conductivity (κ) as a function of temperature: representative data for suspended graphene (red spheres) [63], exfoliated graphene on SiO_2 (light green spheres) [44], exfoliated few-layer graphene on SiO_2 (filled (W/L=5/2 and open (W/L=5/1) olive triangles) [68], graphene grown by chemical vapor deposition on Au/Si_3N_4 (filled orange pentagon) [69], $\sim W/L = 45/244$ nm graphene nanoribbons (GNRs, dark cyan filled hexagons) [70], ~20-nm-wide GNRs (half filled dark cyan hexagon) [11], type IIa diamond (filled blue diamonds) [12], graphite in-plane (filled black squares) [12], ultra-nanocrystalline diamond (open [66] and half-filled [65] blue diamonds), graphite out-of-plane (open black squares) [12].

thermal transport in low-dimensional crystals and the practical tuning of thermal conductivity in low-dimensional crystals by external influences.

Figure 2.5 summarizes selected graphene κ data from the literature to highlight the role of the substrate and edges on thermal transport in graphene. The κ data for bulk single crystal diamond [12], the $\kappa_{||}$ and cross-plane thermal conductivity ($\kappa\perp$) of graphite [12], and the κ of ultra-nanocrystalline diamond (UNCD) [65-66] are included for comparison. The $\kappa_{||}$ for freely suspended graphene ranges from about 2000 to 4000 $Wm^{-1}K^{-1}$[63]. By comparison, the room temperature κ of diamond is $\approx$2200 $Wm^{-1}K^{-1}$ and the $\kappa_{||}$ of graphite is $\approx$1950 $Wm^{-1}K^{-1}$[12]. At the other end of the carbon materials κ spectrum, the room temperature κ of UNCD and the $\kappa\perp$ of graphite are between 6 and 12 $Wm^{-1}K^{-1}$[12, 65-66]. The κ of UNCD is limited by grain boundary

scattering, similar to nanocrystalline semiconductors, while the $\kappa_{\perp}$ of graphite is limited by weak vdW interactions with the adjacent layers. Thermal transport perpendicular to graphene is also limited by weak vdW interactions as previously discussed [38, 60, 67].

The role of a substrate on thermal transport in supported graphene was first reported by by Seol et al. and further substantiated by the Raman thermometry measurements of Cai et al. a short time later [44, 69]. The room temperature κ of substrate supported graphene was found to be $\approx$580 ± 35 $Wm^{-1}K^{-1}$ for mechanically exfoliated graphene on SiO_2, and $\approx$370 +650/−320 $Wm^{-1}K^{-1}$ for graphene grown by chemical vapor deposition and in contact with gold-coated silicon nitride. Jang et al. later reported a further reduction in the room temperature κ of graphene which was encased in e-beam evaporated SiO_2 ($\kappa \approx$160 $Wm^{-1}K^{-1}$) [71]. Electrical thermometry measurements by Bae et al. show an even greater reduction ($\kappa \approx$ 80 $Wm^{-1}K^{-1}$) when SiO_2 supported graphene is patterned into graphene nanoribbons (GNRs) of width $\approx$ 45 nm. Allowing for differences in the quality of the graphene samples, the reduced κ values for substrate supported graphene and GNRs are still in stark contrast to that of freely suspended graphene. These decreases in intrinsic thermal conductivity of "bulk" graphene can be attributed to scattering of graphene phonons by the substrate phonons [44, 72], and an additional phonon scattering contribution from edge roughness in the case of GNRs [70]. Lastly, electrical thermometry measurements performed by Wang et al. show that the $\kappa_{||}$ of few-layer graphene (FLG, n=3) nearly recovers that of bulk graphite ($\kappa_{FLG} \approx$ 1250 $Wm^{-1}K^{-1}$) after just a few atomic layers and when thermal transport in the sample is diffusive [68]. This result suggests the substrate phonons have an associated length scale over which they can scatter phonons in adjacent graphene layers.

We now turn our discussion to thermal transport in CNTs. Figure 2.6 summarizes selected CNT κ data from the literature to highlight the role of 0D crossed CNT junctions on thermal transport in bulk-like CNT films. The κ data for bulk single crystal diamond [12], the $\kappa_{||}$ and $\kappa_{\perp}$ of graphite [12], and the κ of UNCD [65-66] are included for comparison. The data for freely suspended and individual multi-wall and single-wall CNTs (MWCNT and SWCNT, respectively) are also shown. For both individual MWCNTs and individual SWCNTs the data peak near room temperature at $\kappa \approx 3000$ $Wm^{-1}K^{-1}$ [45, 64]. These measurements, as well as earlier predictions [73-74], highlight the intrinsic thermal properties of CNTs, which quickly captured the scientific community's attention. Coupled with the high intrinsic mobility of CNTs

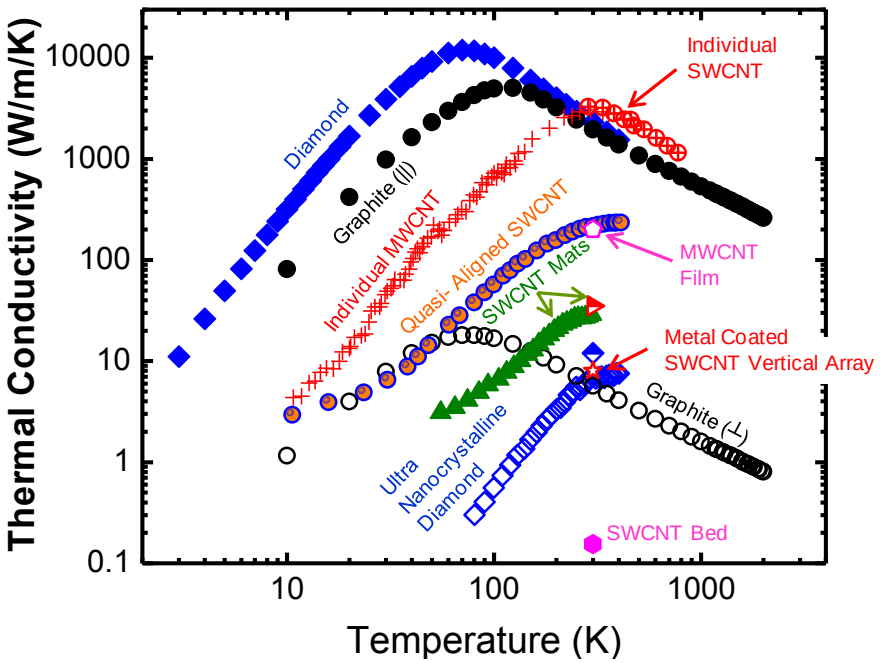

Figure 2.6 Thermal conductivity (κ) as a function of temperature: representative data for an individual single-wall CNT (SWCNT, red circles with crosses) [64], an individual multi-wall CNT (MWCNT, red crosses) [45], quasi-aligned SWCNT films (blue and orange spheres) [78], MWCNT film (open magenta pentagon) [79], SWCNT randomly oriented mats (35 nm thick - filled olive triangles [80], and millimeter-scale films - red half-filled right-facing triangle [81]), a metal-coated vertically aligned array of SWCNTs [82], and a SWCNT 200 to 800 μm thick film/bed (filled magenta hexagon) [83], type IIa diamond (filled blue diamonds) [12], graphite in-plane (filled black squares) [12], ultra-nanocrystalline diamond (open [66] and half-filled [65] blue diamonds), graphite out-of-plane (open black circles) [12].

[75], the high intrinsic κ of CNTs makes them ideal candidates to replace silicon as the channel material in future nanoelectronics devices [1-2, 26, 76]. However, key challenges remain in the selective synthesis, or post synthesis sorting and selective placement of high-density arrays of chirally pure SWCNTs before they can be integrated into future CMOS technologies [77]. Still, the world-wide production capacity of CNTs has reached an estimated 5 kilotons/year, indicating the demand for CNTs is growing in commercial sectors outside the nanoelectronics industry [26].

In particular, CNT network thin film transistors (CN-TFTs) are finding widespread applications in macroelectronics with a wide range of applications such as flexible electronics, chemical sensors, e-clothing, and antennas [84-86]. Recent work by our group and others has shown that the morphology of the CNT network and the low thermal conductance ($\approx$5 MW $m^{-2}K^{-1}$) of crossed CNT junctions limit the performance and high-field thermal reliability of CN-TFTs [10, 87-89]. Electrical thermometry measurements performed on crossed MWCNTs by Yang *et al*. along with thermal conductivity measurements on bulk CNT beds by Prasher et al. also revealed the high thermal resistance of crossed CNT junctions (Figure 2.6) [83, 90]. In the latter case, the thermal conductivity of the CNT bed is as low as 0.15 $W^{-1}K^{-1}$, near that of amorphous carbon. These results provide insight into the wide spread in the measured thermal conductivity of CNT based nanomaterials seen in Figure 2.6.

Hone et al. reported some of the first measurements of thermal conductivity of randomly oriented bulk SWCNT mats. They found the room temperature κ was $\approx$30 $Wm^{-1}K^{-1}$[81], with an estimated Λ of 0.5 to 1.5 μm, which was on the order of the length of individual SWCNTs within the mat. Therefore, they suggested boundary scattering (presumably at crossed SWCNT junctions) could play a role in the observed low κ. Later infrared bolometric measurements by

Itkis, et al. on randomly oriented SWCNT mats found a comparably low κ, which they attributed to CNT junctions. They estimated the CNT junctions accounted for ≈98% of the total thermal resistance of the SWCNT mat (Figure 2.6) [80]. These findings are substantiated by earlier measurements on quasi-aligned SWCNTs [78] and MWCNT films [79], which showed an enhanced thermal conductivity at room temperature ($\kappa_{||} \approx 220$ $Wm^{-1}K^{-1}$) as compared to randomly oriented SWCNT mats. Aligned CNTs and larger diameter CNTs are expected to have a greater contact area between neighboring CNTs, increasing the area for heat flow across CNTs. Molecular dynamic simulations by Zhong and Lukes also show thermal transport across contacting CNTs depends on the contact area [91]. It is then intuitive to suggest that vertically aligned arrays of CNTs, where thermal transport occurs along the individual tube axes, should recover the intrinsic properties of the individual CNTs within the array. However, thermoreflectance measurements by Panzer et al. indicate the lower bound for the thermal conductivity of 28 μm long vertically aligned CNT arrays is ≈8 $Wm^{-1}K^{-1}$[82]. The low κ in such arrays is attributed to the high thermal contact resistance between the CNTs and their supporting substrate and contact metal.

2.3 Conclusions

In summary, the use of nanoscale devices and materials in current and future integrated circuit technology is problematic in that the length scales of the electron devices are approaching the wavelengths and mean free paths of the carriers responsible for heat transport in the device. This aggressive scaling is expected to have significant impacts on power dissipation and device reliability and variability for future nanoelectronic devices. Moreover, the role of defects and nanoscale dimensions on device reliability and transport is an important area of study in order to fully understand the best applications for emerging nanomaterials. These problems require the

development of new and accurate metrology methods, along with computational models, to further understand reliability and power dissipation in nanoscale devices.

To this end, this study investigates novel aspects of device reliability and power dissipation in CNT transistors, as well as the role of defects on chemical sensing and thermal transport in graphene grown by chemical vapor deposition (CVD). A pulsed technique to suppress hysteresis in CNT transistor transfer characteristics is demonstrated. As hysteresis is reduced, both forward and backward gate voltage sweeps move towards a common, unique central transfer characteristic which reveals the "true" device mobility and threshold voltage. Infrared thermal imaging is used to image power dissipation in CNT-TFTs, and to develop a compact thermal model to extract the role of CNT junctions on power dissipation. The chemical sensitivity of graphene grown by CVD on copper foils is found to depend on linear defects in the film. Lastly, thermal transport in CVD graphene is investigated using a novel electrical thermometry platform. The thermal conductivity is found to be lower than that of substrate supported exfoliated graphene due to grain boundary and substrate phonon scattering. The thermal conductivity of layer-by-layer assembled graphene films increases significantly, showing, for the first time, how thermal transport can be tuned one atomic layer at a time in vdW solids.

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CHAPTER 3

REDUCTION OF HYSTERESIS IN CARBON NANOTUBE FIELD-EFFECT TRANSISTOR MOBILITY MEASUREMENTS

3.1 Hysteresis in Carbon Nanotube Field-Effect Transistors

Carbon nanotube field effect transistors (CNT FETs) are candidates for future nanoelectronics due to their ability to carry large current density and their high mobility, greater than 10^9 A/cm^2 and 10^4 cm^2/V·s respectively [1-3]. In many studies, CNT FETs are grown or dispersed onto an insulator and back-gated by a silicon substrate. Hysteretic behavior in the drain current (I_D) with gate-to-source voltage (V_{GS}) transfer characteristics is often observed, and varies depending on sweep direction, sweep rate, and environmental conditions. This behavior is typically attributed to charge trapping by surrounding water molecules or charge injection into the dielectric substrate [4-11]. Sweeping $V_{GS} > 0$ typically shifts the threshold voltage (V_T) up because of charge screening from injected electrons into trap sites. Similarly, sweeping $V_{GS} < 0$ induces hole injection into the CNT surrounding, and the threshold voltage is shifted down [12]. This leads to the observed "open eye" characteristics when continuous (DC) I_D-V_{GS} measurements are made (see, e.g. [4-8]), which causes uncertainty in measured threshold voltage, conductance, and mobility. In a DC sweep the charges remain trapped until the gate polarity is switched [13]. Although this hysteretic behavior can be exploited to create nonvolatile memory devices [12, 14-15], it is often unclear which electrical characteristics should be used to extract carrier mobility and threshold voltage for transistor applications. This uncertainty has lead to large discrepancies (>10×) in reported mobility values because both the reverse [1] and

Table 3.1 Mobility values reported for various CNTs in the literature

μ ($cm^2V^{-1}s^{-1}$)	***d* (nm)**	***L* (μm)**	**V_{GS} Sweep or Hysteresis Reduction Method**
Ballistic	3	0.3	*PMMA passivated [3]
79,000 ± 8,000	3.9	325	Reverse sweep [1]
5,000 – 20,000	<5	4000	*Not reported [16]
16,000	4	4	Forward [2]
4,000	3	3	*PMMA passivated [3]
2,500	1.5	10	Forward sweep [2]
1,000 - 4,000	1 to 4	1 to 3	*Vacuum [17]
20	1.6	0.3	*Not reported [18]
600 - 8,000	Not reported	3	*PEI doped [19]

Polymer coatings or vacuum conditions have sometimes been used to reduce hysteresis when extracting mobility [3, 17, 19]. In a few studies the direction of the sweep used for mobility calculation is unavailable [16, 18].

forward [2] I_D–V_{GS} sweeps have been used to extract mobility, and in some studies the V_{GS} sweep direction was not reported (Table 3.1).

In this work, we describe a pulsed measurement technique to suppress hysteresis in single-wall CNT FET transfer characteristics, and subsequently use it to extract the effective mobility value for the CNTs tested without gate screening effects. The approach is quite general and could be applied to CNTs on other dielectrics, substrates, and polymers or to other nanoscale conductors (e.g. graphene) where unwanted hysteretic behavior is often observed. We find that increased off times between gate voltage pulses reduce measured hysteresis, and the transfer characteristics move towards a common, unique curve revealing a single value for the device mobility. The direction of the hysteresis reduction may also provide insight into the type of traps affecting device performance. By varying the pulse width and duty cycle in our measurements over a wide range (1 ms to 10 s), we also extract the relaxation times associated with environmental charge trapping at various temperatures from 80 to 453 K, in air and in vacuum. We adapt a tunneling front model [20-22] to extract the associated trap depths affecting

hysteresis in our measurements. Finally, we investigate the error in extracted carrier mobility in CNTs between the (unique) pulsed and (ambiguous) DC gate voltage measurements.

3.2 Experimental Methods

To fabricate the devices used in this study, we begin by removing the native oxide from a bare highly doped (p+) Si wafer in a HF solution, followed by a 15 minute clean in a 7:1 H_2O_2:H_2SO_4 (Piranha) solution. Approximately 70 nm of dry thermal SiO_2 is grown at 1150 °C. Next, about 1 nm of Fe is deposited onto lithographically defined catalyst areas using standard lithography and electron-beam (e-beam) evaporation. Carbon nanotubes are grown in an Atomate chemical vapor deposition (CVD) system by annealing the substrate at 900 °C in an Ar environment for 30 minutes followed by CNT growth at 900 °C under CH_4, C_2H_4, and H_2 flow (~ 50:1:30). Metal pads are lithographically aligned to the pre-patterned catalyst and deposited by e-beam evaporation (1 nm Ti/ 40 nm Pd). The electrode pads are defined by lift-off in MicroChem Remover PG. The contacts are annealed at 300 °C in an Ar environment for 30 minutes. The highly doped (p+) silicon substrate served as the back gate, and CNTs were

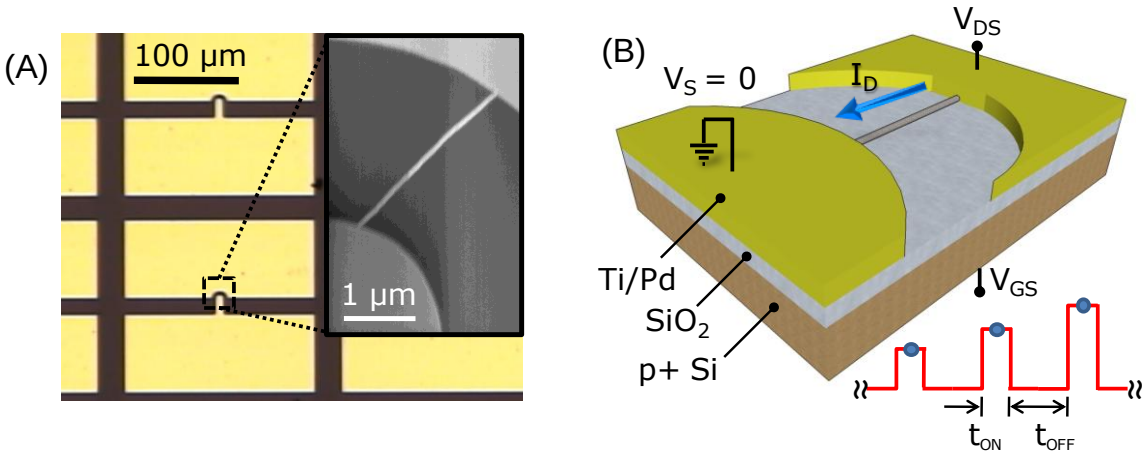

Figure 3.1 (A) Top view optical image of typical CNT devices used in this work. Metal pads are Ti/Pd, 0.5/40 nm thickness. Nanotubes were grown by CVD using Fe catalyst on top of ~70 nm of SiO_2. The devices are back-gated with the highly doped (p+) Si wafer beneath. Semicircular electrodes are used for tighter control of nanotube device length. **(inset)** SEM image of typical device. **(B)** Schematic of device with one active connection and pulsed gate voltage.

exposed to ambient environment from above, as shown in Figure 3.1 [23].

CNT diameter (d) and length (L) were measured by atomic force microscopy (AFM), and scanning electron microscopy (SEM) (inset Figure 3.1 (A)). Transfer characteristics were measured using a Keithley 2612 dual-source measuring unit, at constant V_{DS} = 50 mV, while performing a pulsed sweep of V_{GS} between ±10 V (inset Figure 3.1 (B)). Pulsed I_D-V_{GS} characterization of CNT FETS is achieved through a custom script written in the Lua language, which is based on the Keithley 2612 instrument default I_D-V_{GS} characterization script. The user-defined V_{GS} sweep is applied in a pulsed linear fashion with a base voltage of V_{GS} = 0 V. Communication with the instrument is achieved through a LabView interface and the model KUSB-488A IEEE-488.2 USB-to-GPIB interface adapter. The gate voltage pulse period was varied from 2 ms to 10 s with the pulse width held constant at 1 ms. A constant pulse width was used because no significant dependence of hysteresis on it was found in the range of 250 μs to 1 ms. Measurements were made under varying conditions and temperatures. The devices in this study had diameters ranging from $d \approx$ 1.6 to 3.8 nm, and channel lengths $L \approx$ 2 to 7.5 μm.

3.3 Hysteresis Reduction

The hysteresis gap (ΔV_T) is defined as the difference in threshold voltage between the forward and backward V_{GS} sweeps, as determined by the linear extrapolation method (Figure 3.2 (A)) [24]. Hysteresis dependence of pulsed measurements is compared in air and vacuum (~10^{-5} torr) at room temperature for two CNTs with similar length and diameters, $d \approx$ 2.1 nm (Figures 3.2 (A) and (B)) and $d \approx$ 1.7 nm (Figures 3.2 (C) and (D)). Hysteresis is found to be reduced by increasing the length of the pulse off time (t_{OFF}). In air, hysteresis is reduced by up to 75% (Figure 3.2 (A)) when t_{OFF} is increased from 1 ms to 10 s. In vacuum, hysteresis is nearly eliminated (Figure 3.2 (D)) when t_{OFF} is increased from 1 ms to 10 s. Furthermore, hysteresis

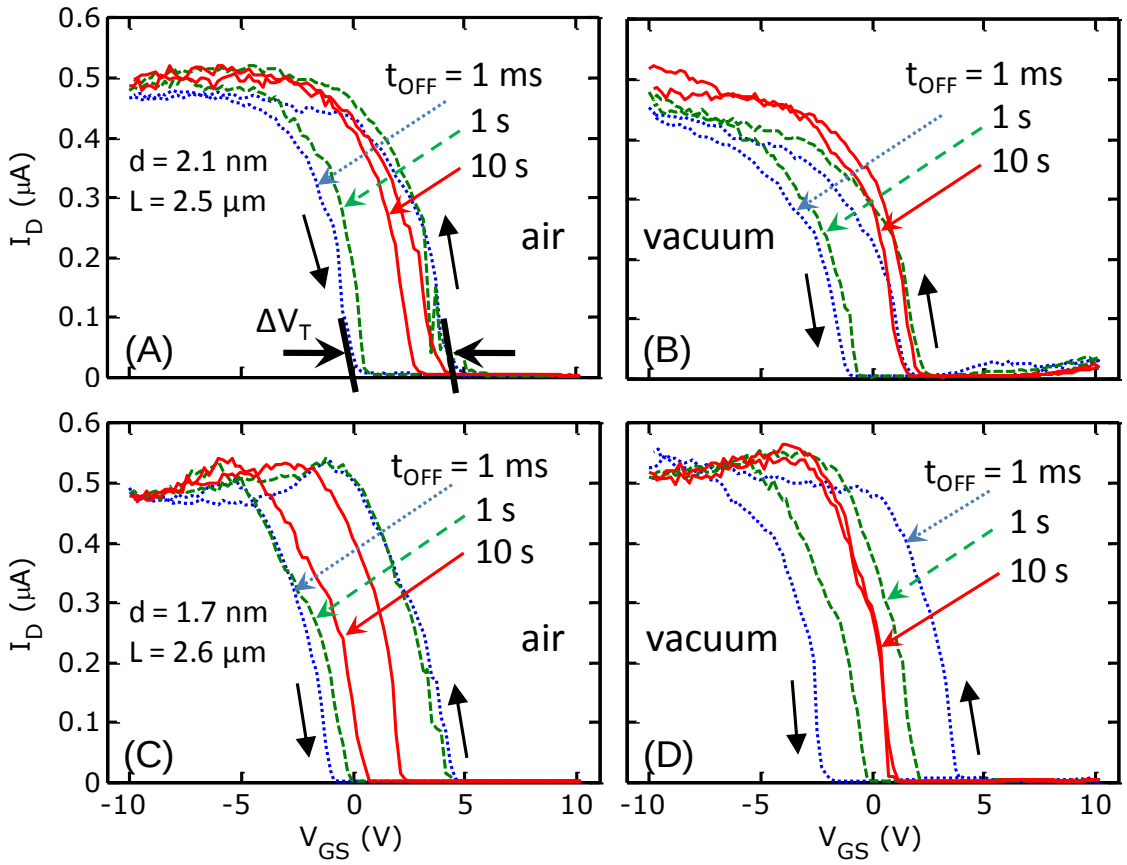

Figure 3.2 (A) Typical I_D-V_{GS} transfer curves for a device with $d \approx 2.1$ nm in air and **(B)** in vacuum (~10^{-5} torr) at room temperature. The hysteresis gap (ΔV_T) is defined as the difference between the forward and reverse sweep threshold voltage. The hysteresis loop indicates charge trapping into the substrate [12]. **(C)** Typical I_D-V_{GS} transfer curves for a device with $d \approx 1.7$ nm in air and **(D)** in vacuum at room temperature. In all cases hysteresis is reduced by increasing t_{OFF} of the applied V_{GS} pulses.

reduction in vacuum is more pronounced at shorter off times for the device with $d \approx 2.1$ nm, indicating charge injection into the substrate affects hysteresis less than charge trapping by surrounding water molecules (which partially desorb in vacuum) [6] for this device. However, for the device with $d \approx 1.7$ nm, the exposure to vacuum has no effect on the hysteresis at shorter off times, possibly due to reduced surface area for water adsorption and the increased electric field (which scales roughly as ~1/d) at the CNT/SiO_2 interface. For this device, charge injection into the substrate is most likely the dominant cause of hysteresis.

Figure 3.3 (A) shows measurements made in air at temperatures from 293 to 453 K, indicating the rate of hysteresis reduction (ΔV_T) with t_{OFF} increases with temperature. This

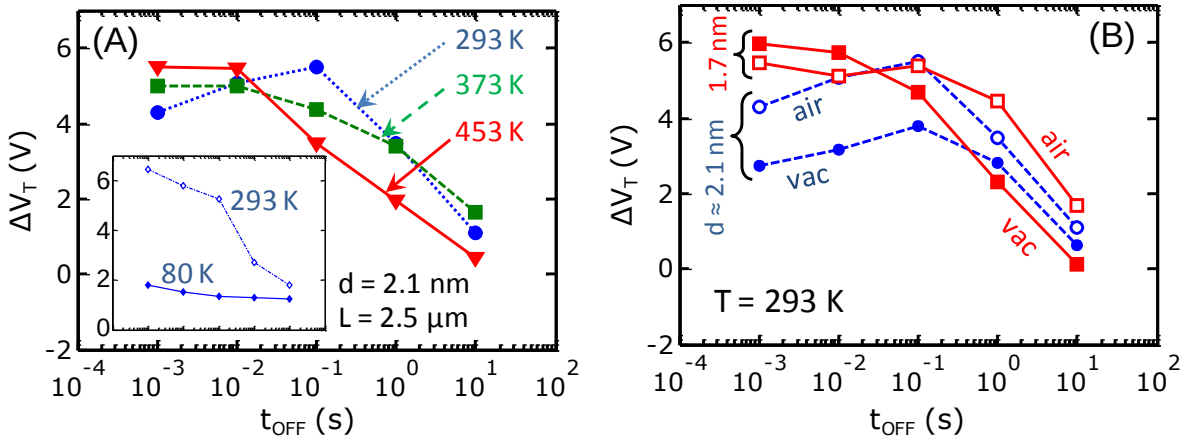

Figure 3.3 (A) Hysteresis gap (ΔV_T) vs. pulse off-time (t_{OFF}) for the device in Figure 3.2 (A) at 293 K (●), 373 K (■), and 453 K (▼) in air. Pulsed measurements are more effective in reducing the hysteresis at higher temperatures. Inset shows nearly constant $\Delta V_T \approx 1.5$ V with various t_{OFF} in vacuum at low temperature (80 K). **(B)** ΔV_T vs. t_{OFF} for the devices in Figures 3.2 (A) and (B). For both the hysteresis reduction is greatest at $t_{OFF} > 100$ ms, indicative of trap relaxation times.

temperature dependence suggests reduced charge trapping by the surrounding water molecules, and faster relaxation times of trapped charge at higher temperature. At low temperature in vacuum (80 K, in Figure 3.3 (A) inset) we find hysteresis is nearly constant at $\Delta V_T \approx 1.5$ V, similar to the behavior observed with DC measurements by Vijayaraghavan et al. [10]. Figure 3.3 (B) illustrates the dependence of ΔV_T on t_{OFF} at room temperature in air and under vacuum. In both Figures 3.3 (A) (in air) and (B) (in vacuum) at short t_{OFF} (< 100 ms), there is no significant dependence of ΔV_T on t_{OFF}. However, at higher t_{OFF} there is a rapid decrease in hysteresis as the trapped charge surrounding the CNT has adequate time to relax during the off part of the gate voltage pulses. This indicates the typical relaxation (detrapping) times of injected charge into the substrate are greater than 100 ms.

3.4 Discussion

We can gain insight into the distribution of trap depths affecting hysteresis, i.e. those with tunneling times approximately between 0.01 and 10 s, by numerically examining the charge tunneling and trapping process. We first calculate the electric field from the CNT into the SiO_2:

$$F(x) = \frac{V_{GS}}{x \ln\left(2\frac{t_{OX}}{r}\right)}; x \geq r \tag{3.1}$$

where t_{OX} is the SiO_2 thickness, r is the CNT radius, and x is the distance from the center of the CNT into the SiO_2, e.g. $x_{max} = t_{OX} + r$ [25]. Unlike in a parallel plate capacitor where the electric field is constant, this field can be very high near the CNT/SiO_2 interface given the extremely small CNT radius, even for only a few volts applied across the SiO_2 dielectric. The band edge diagram of the CNT/SiO_2 interface is schematically displayed in the Figure 3.4 (A) inset. The barrier height associated with tunneling, Φ, depends on CNT diameter through

$$\Phi \approx \varphi_{CNT} - \chi_{SiO_2} - \frac{E_G}{2} \tag{3.2}$$

where $\varphi_{CNT} \approx 4.7$ eV is the CNT work function, $\chi_{SiO_2} \approx 0.95$ eV is the SiO_2 electron affinity, and $E_G \approx 0.84/d$ is the CNT band gap with the diameter d given in nanometers [21, 26-27]. The tunneling time constant can then be written as

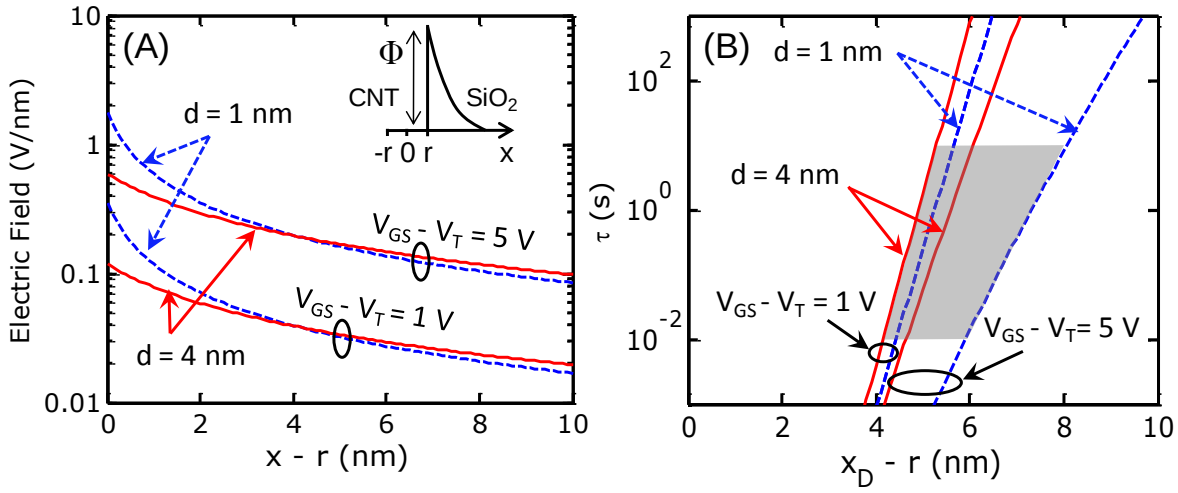

Figure 3.4 (A) Calculated electric field near the CNT/SiO_2 interface for CNTs of diameter $d \approx 1$ nm (dashed blue) and ≈ 4 nm (solid red line) at gate voltage overdrive V_{GS}-$V_T \approx 1$ and 5 V. **(B)** Calculated tunneling time vs. trap depth from the CNT/SiO_2 interface for CNTs of $d \approx 1$ and 4 nm at V_{GS}-$V_T \approx 1$ and 5 V. The estimated trap depth window affecting hysteresis in our measurements is shown as the shadowed region.

$$\tau = \tau_0 \exp\left\{ \int_r^{x+r} \frac{(2m^* x')^{\frac{1}{2}}}{\hbar} \left[\frac{\Phi}{x'} - qF(x') \ln\left(\frac{x'}{r} \right) \right]^{\frac{1}{2}} dx' \right\} \tag{3.3}$$

where $m^* \approx 0.42 m_0$ is the effective tunneling mass in SiO_2, x_D is the trap depth, m_0 and q are the electron mass and charge, respectively, and $\tau_0 \approx 6.6 \times 10^{-14}$ s is a characteristic time constant fitted against previous tunneling front model experiments in SiO_2 [20-22]. From Equation 3.3 we can see that as x_D approaches the CNT/SiO_2 interface, the time scale τ approaches τ_0.

The effective potential ($V_{GS,eff}$) experienced by the CNT can in practice be different from that applied to the gate electrode. This difference is in part due to charge screening by the adsorbed water molecules on the surface of the CNT/SiO_2, and to the injected charge during measurements. Therefore, the simple model described in Equations 3.1 to 3.3 above is used to estimate the upper bounds of the trap depths (x_D) associated with relaxation times between τ = 0.01 and 10 s [28]. A more rigorous approach would self-consistently take into account the charge screening, potential (field) profile, and tunneling process, see e.g. [28]. This model is shown in Figure 3.4 for CNTs of diameter d = 1 and 4 nm with an effective potential $V_{GS,eff}$ = 1 and 5 V. As expected, the field is greater for the smaller diameter tube near the CNT/SiO_2 interface ($x - r = 0$), shown in Figure 3.4 (A). As a result we expect CNTs of smaller diameter to populate traps farther away from the CNT/SiO_2 interface, as shown in Figure 3.4 (B) where the scale is set to expand the area of interest. Using this model we estimate the trap depths for the time constants τ = 0.01 and 10 s to correspond roughly to $x_D \approx 4$ and 5 nm, respectively, for a CNT FET with d = 4 nm at $V_{GS,eff}$ = 1 V. For a CNT FET with d = 1 nm and $V_{GS,eff}$ = 5 V, the corresponding trap depths for time constants τ = 0.01 and 10 s are 6 and 8 nm respectively. As the trap depth approaches the CNT/SiO_2 interface, the model correctly converges to τ_0 for all cases. The model suggests a dependence of measured hysteresis on CNT diameter. However,

experimentally we do not find a clear dependence of hysteresis on either CNT diameter or length after comparing ΔV_T from the DC transfer characteristics of nineteen CNT FETs. We attribute this lack of diameter dependence to variability in the SiO_2 surface roughness between different samples [15], to defects in the CNTs measured, and to ambient conditions which cannot be precisely controlled at the atomic scale of the CNT interface during measurement. However, it is evident that the pulsed measurements described in this work yield consistent, reproducible results (i.e. hysteresis reduction) in spite of such variability between CNT samples, and the relatively straightforward approach should make it applicable to a wide range of nanostructures with inherent variability, such as graphene, nanowires, or molecular electronics.

We note the direction of the hysteresis collapse may provide some insight into the trap

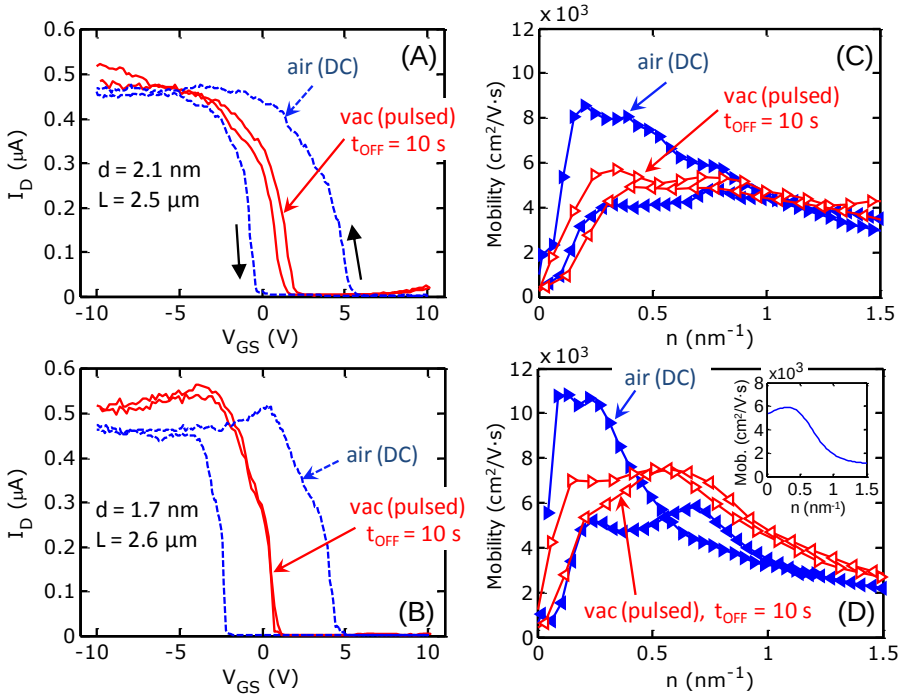

Figure 3.5 (A) Typical DC I_D-V_{GS} transfer curves for the device with diameter $d \approx 2.1$ nm in air (dashed) and pulsed under vacuum conditions (solid). **(B)** Similar data for a device with diameter $d \approx 1.7$ nm in air (dashed) and pulsed under vacuum conditions (solid). **(C)** Corresponding mobility extraction for the device in (A) and **(D)** for the device in (B). Rightward (filled) triangles indicate mobility from forward V_{GS} sweep and leftward (open) triangles from reverse sweep. Inset in (D) indicates good agreement of multi-band mobility simulations from our recent work [29] with the mobility extraction from pulsed measurements.

sites being populated. For example, hysteresis collapse towards more positive gate voltage (Figures 3.2 (A) and (C)) could be indicative of hole traps depopulating. Hysteresis collapse towards center (Figures 3.2 (B) and (D)) could indicate an equal number of hole and electron traps depopulating. Hysteresis collapse toward negative gate voltages could indicate electron traps depopulating. In addition, we note that typical oxides have trap densities ranging from 10^{10} to 10^{13} cm^{-2} [30] which correspond to only 1 to 600 traps for typical CNTs in our study (~3 μm length and ~2 nm diameter). Thus, variation in the oxide quality on our test chips can strongly influence the electrical properties of CNT devices.

Before concluding, we compare the effective mobility extracted from the forward and reverse DC sweeps in air, with the mobility extracted from pulsed measurements with t_{OFF} = 10 s under vacuum. This extraction is done for the devices with similar length and diameters $d \approx$ 1.7 nm and 2.1 nm in Figure 3.5. The effective mobility is $\mu_{EFF} = \frac{GL}{qn}$ where $n = \frac{C'}{q(V_T - V_{GS})}$ is the carrier density per unit length obtained from the experimental data, $G = \frac{I_D}{V_{DS} - I_D R_C}$ is the drain conductance at V_{DS} = 50 mV, and $C' = \frac{2\pi\varepsilon}{\ln\left(\frac{2t_{OX}}{r}\right)}$ is the CNT capacitance per unit length with $\varepsilon \approx 2.2\varepsilon_0$ for CNTs on SiO_2 to effectively account for fringing fields [25]. R_C is the contact resistance, estimated from measurements at low field (R_{LF}) such that $R_C = R_{LF}$-R_0, where R_0 is the intrinsic resistance of the CNT, which depends on L and the acoustic phonon mean free path, $\lambda_{AP} \approx 280d$ as described in our recent work [29]. For the device with $d \approx$ 1.7 nm and $L \approx$ 2.6 μm, we obtain $R_0 \approx$ 42 kΩ and for the device with $d \approx$ 2.1 nm and $L \approx$ 2.5 μm we obtain $R_0 \approx$ 34 kΩ. The V_T used in calculating μ_{EFF} is determined by finding the gate voltage at a specified threshold

drain current (I_T), such that $I_T \approx \frac{G}{G_0} < 0.001$. Here, $G_0 = \frac{4q^2}{h}$ is the quantum conductance of four CNT channels [29].

We find that at longer pulse t_{OFF} times, there is less discrepancy between forward and backward sweeps, and the extracted mobility approaches a common value (Figures 3.5 (C) and (D)). Moreover, we find the extracted mobility varies by approximately a factor of two between the forward and backward DC sweeps in air, highlighting the inadequacy of extracting mobility from a DC sweep. However, when measured with the pulsed technique in vacuum, the error in extracted mobility between the forward and backward V_{GS} sweep is reduced to approximately 10% for the device with $d \approx 2.1$ nm and completely eliminated in the case of the device with $d \approx 1.7$ nm. It is interesting to note that the extracted μ_{EFF} from the pulsed measurement technique lies between that extracted from the forward and reverse DC sweeps. This suggests that Coulomb scattering due to trapped charge has a weaker effect on the CNT mobility than acoustic phonon scattering. Furthermore, we note that in both cases the mobility initially increases and then decreases with carrier concentration (n), peaking at $n \approx 0.5$ to 1 carriers/nm. This result is precisely consistent with the inverse dependence of CNT mobility on the density of states (DOS), as the DOS first decreases when the Fermi level (EF) moves away from the edge of the first sub-band, and then increases as EF enters the second sub-band, leading to a decrease in mobility as a new scattering channel becomes available. A quantitative model for the behavior of CNT effective mobility in the presence of multiple sub-band conduction was recently given by our work in [29]. This model is shown in the Figure 3.5(D) inset, which displays good quantitative agreement with the mobility extraction from pulsed measurements.

3.5 Conclusions

We have described a pulsed measurement method which eliminates unwanted hysteresis of CNT FETs in air and under vacuum conditions. By varying the off time of the pulses we find the relaxation time of the trapped charge affecting hysteresis to be between 100 ms and 10 s. We also present a simple tunneling front model to extract the upper bounds of the charge trap depths, estimated to between 4 and 8 nm for CNTs of diameter 4 nm and 1 nm, respectively. The effect of hysteresis on mobility extractions from the forward and reverse DC gate voltage sweeps is determined, and it is shown that long pulse intervals at high temperature and under vacuum result in the extraction of a more consistent mobility value for CNTs. The approach presented here opens the door and could also be applied for more careful evaluations of other nanostructures with inherent variability and trapped charge effects, including graphene, nanowires, and molecular devices.

3.6 References

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CHAPTER 4

IMAGING DISSIPATION AND HOT SPOTS IN CARBON NANOTUBE NETWORK TRANSISTORS

Random networks of single-wall carbon nanotubes (CNTs) are of interest for integrated circuits [1] and display drivers [2] on flexible or transparent substrates, particularly where they could exceed the performance of organic or amorphous thin film transistors (TFTs). A common problem of such TFTs is that they are often placed on low thermal conductivity substrates like glass or plastics, leading to self-heating effects [3] and reduced reliability [4], topics not yet explored in carbon nanotube network (CNN) transistors. An additional concern with CNNs is that performance and reliability may be limited by high electrical [5-7] and thermal [8-11] inter-tube junction resistances. For CNNs this could result in large temperature increases (hot spots) at the CNT junctions which greatly exceed the average temperature of the device channel.

4.1 Device Fabrication and Experimental Setup

In this study, we use infrared thermal imaging [12] and electrical breakdown thermometry [13] to investigate power dissipation in CNNs. We show that under high bias stress, devices fail with a minimal rise in average device temperature. Furthermore, we show power dissipation can be localized at so-called "hot spots" in the CNN, which can be detrimental to TFT applications. In addition, we introduce a model to extract the average thermal resistance between CNNs and the substrate (R_C), as well as the CNT junction thermal resistance (R_J). Our results indicate that the latter is the key limiting factor in CNN performance, dissipation, and reliability. The CNNs used in this study were grown using an Etamota chemical vapor deposition (CVD) system. Low-density CNNs were grown using ferritin catalyst. High-density CNNs were grown by depositing

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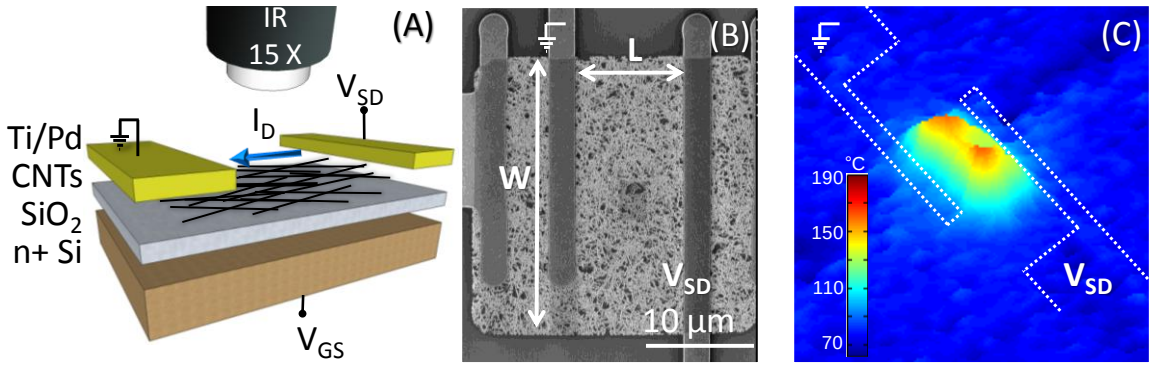

Figure 4.1 (A) Schematic of CNN device and experimental setup. **(B)** Scanning electron microscopy (SEM) image of a high density CNN device ($L \approx 10$ µm, $W \approx 25$ µm) before IR imaging and CNT breakdown. **(C)** Temperature profile of the device in (B) measured at a power $P \approx 25$ mW, in air, with background temperature $T_0 = 70$ °C. The non-uniform temperature profile is indicative of percolative transport in such CNN devices

~ 2 Å Fe catalysts via e-beam evaporation. In both cases the catalysts were placed onto 90 nm SiO_2 on highly n-doped Si which acts as a back gate. Substrates were annealed at 900 °C in an Ar environment, followed by CNT growth for 15 minutes under CH_4 and H_2 flow. Standard photolithographic techniques were used to pattern the CNN by oxygen plasma etching, and the electrodes (Ti/Pd 1/40 nm) by lift-off, as shown in Figure 4.1. Electrical and thermal measurements were performed using a Keithley 2612 dual channel source-meter and a QFI InfraScope II infrared (IR) microscope, respectively [14]. The highly n-doped Si also acts as a back gate. All infrared (IR) thermometry measurements are performed at a background temperature $T_0 = 70\ ^oC$ for optimum IR microscope sensitivity [9]. To minimize uncertainty in our analysis, we set the back-gate such that both metallic and semiconducting CNTs are turned "on" ($V_G < -15$ V).

4.2 Infrared Imaging

Before performing IR measurements of the CNN-TFTs, we acquire a reference radiance image which is used to calculate the emissivity at each detector pixel. This measurement is done without biasing the device at a background temperature $T_0 \sim 70$ °C for optimum IR microscope

sensitivity. We then measure the background temperature with the IR scope to confirm the setup, verifying all pixels measure T_0. We acquire IR images under increasing source-drain bias (V_{SD}) conditions, and, surprisingly, we find the imaged channel temperature increases very little, even at high V_{SD} approaching device breakdown. For instance, the maximum temperature rise imaged in the high-density CNN shown in Figures 4.1(B) and 4.1(C) is $\Delta T \approx 30$ °C at a power $P = I_D V_{SD}$ = 25 mW. Moreover, the temperature in the channel is non-uniform, with distinct hot spots forming in the CNN depending on the local density variations and the CNT percolative pathways.

Lower density CNNs (Figure 4.2 (A)) do not provide as strong a thermal signal under IR

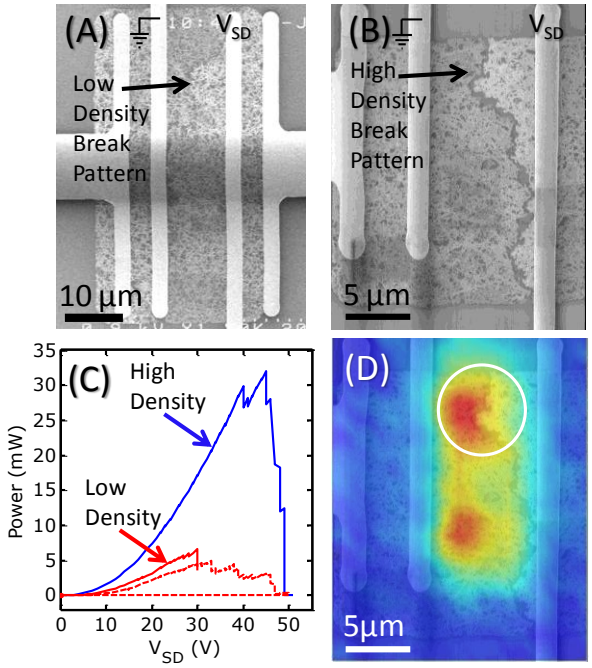

Figure 4. 2 (A) SEM image of a low-density device ($L \approx 10$ µm, $W \approx 50$ µm). **(B)** Measured power vs. applied voltage up to breakdown of low-density device from (A) and high-density device from (C). In both cases, large drops in power indicate breaking of the CNT film. The dashed line shows the second sweep of the low-density device, taken after the initial test was stopped at the V_{SD} = 30 V break. Small arrows indicate sweep directions. **(C)** SEM image of the high-density device from Figure 4.1 (B) after breakdown. **(D)** Measured temperature profile just before breakdown, at P = 25 mW (from Figure 4.1 (C)) overlaid onto the SEM from (C). The circled breakdown location bears the imprint of the adjacent hot spot. Although the breakdown occurs too fast to be imaged by our IR camera, we suspect the initial CNN break occurred at the upper hot spot, leading to a rerouting of the current pathways to cause the subsequent full break.

imaging [14], but facilitate analysis because the number of CNT junctions can be readily examined and counted by SEM, as will be shown below. The power-voltage characteristics (*P-V)* of low- and high-density CNNs biased up to the breakdown point are shown in Figure 4.2 (B). In both cases we note a sharp drop corresponding to a breakdown power P_{BD} ~ 6.7 and 30 mW for the low- and high-density devices, respectively. This signals a catastrophic break of the CNN, also noted when the *P-V* characteristic of the low-density device cannot be recovered on a subsequent sweep (dashed line in Figure 4.2 (B)). In addition, we note the breakdown location of the film from Figure 4.2 (C) bears the imprint of the hot spot formation in the overlaid image of Figure 4.2 (D).

4.3 Network Analysis and Thermal Model

We now focus on the low-density device to better understand how measured breakdown power (P_{BD}) corresponds to the breakdown temperature (T_{BD}) and the temperature measured by IR microscopy. To this end, we develop a thermal resistance model as shown in Figure 4.3 (A). In general, the power and temperature rise of a device are related through the thermal resistance [15], here $T_{BD} - T_0 = P_{BD} \cdot R_{TH}$ at breakdown. We assume the well-known T_{BD} = 600 °C for

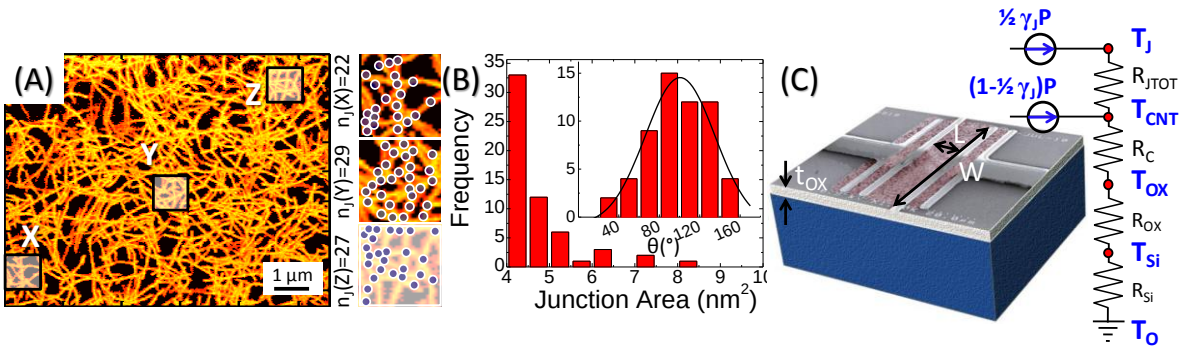

Figure 4.3 (A) SEM image of part of the low-density CNN (from Figure 4.2 (A)) imported to Matlab and used for analysis of the total CNN length (L_C), area (A_C), and junction density (n_J). The highlighted portions of the SEM are magnified and the number of CNT junctions (dots) are counted to obtain averages. **(B)** Histogram of average CNT junction area A_J and (inset) angle of intersection θ. **(C)** Simple thermal resistance model used to evaluate CNN dissipation and estimate the various temperature differences, including from CNT junctions.

CNTs in air [16], recalling that T_0 = 70 ^{o}C was used in this study [12]. To simplify the analysis we assume uniform power dissipation across the CNN, although we know this is not strictly the case due to the percolative transport, as well as the imaged temperature profile (Figure 4.2 (D)). However, as we will show, this allows us to determine a quantitative lower bound on the CNT junction resistance, R_J.

We note that power is dissipated both at the CNT junctions and along the length of the CNTs in contact with the SiO_2. This observation requires knowledge of the junction area fill factor (γ_J) with respect to the CNN area (A_C) in order to develop a thermal model. To determine γ_J, we first extract the area fill factor of the network (γ_C) by analyzing SEM images of the CNN. The images are imported to a matrix form in Matlab [17], and a threshold contrast is chosen to designate areas occupied by CNTs [14]. A typical processed image is shown in Figure 4.3 (B). The ratio of matrix elements with values above threshold to the total number of matrix elements is ~0.72, which is a significant overestimate of the true areal coverage (γ_C) because CNT diameters appear much larger under SEM, 30 < $\langle d' \rangle$ < 80 nm. Choosing $\langle d' \rangle \approx 50$ nm, we can estimate the total length of CNTs in the network, $L_C \approx 7.2$ mm, from $\gamma_C = \langle d' \rangle \sum \frac{L_C}{A}$, where the device area is $A = W \times L$. The actual area of the CNN is $A_C \approx d \times L_C \approx 14.4\ \mu m^2$, with a true area fill factor $\gamma_C \approx 0.03$, where $d \approx 2$ nm is the actual CNT diameter, averaged from atomic force microscopy (AFM) analysis [14]. (We return to the effect of variability in $\langle d' \rangle$ from SEM analysis after extracting R_J below.)

We estimate the total CNT-CNT junction area as $A_{JTOT} \approx A_J \times (n_J \times A)$, where A_J is the average area of a CNT junction and n_J is the junction density per device area A. We note A_J depends on the angle of intersection (θ) of CNTs in the random network, i.e. $A_J = \frac{d^2}{\sin(\theta)}$. Here

we use image analysis software [17-18] to determine average values for n_J, A_J, and θ, as shown by the histograms in Figure 4.3 (C). We find $A_J = 4.69 \pm 0.93$ nm^2, $\theta = 98 \pm 28°$, and $n_J \approx 26$ μm^{-2}. Thus, the density of junctions in the network $\gamma_J = A_{JTOT}/A_C = 0.0042$, which completes the inputs needed for the thermal model in Figure 4.3 (A). We note that in CNNs, n_J is partly dependent on CNN density and CNT length [6]. Therefore, when applying our thermal model to other device structures, it is important to carefully estimate n_J for specific device geometries and CNN

density.

To find the total thermal resistance [15] of the CNN, we include the Si substrate thermal resistance $R_{Si} = \frac{1}{2\kappa_{Si} A^{\frac{1}{2}}}$, the SiO_2 thermal resistance $R_{OX} = \frac{t_{OX}}{\kappa_{OX} A_C}$, and the CNT-$SiO_2$ thermal boundary resistance of the network $R_C = \frac{1}{gL_C}$. Here $t_{ox} = 90$ nm, $\kappa_{ox} \approx 1.4$ W m^{-1} K^{-1}, $\kappa_{Si} \approx 100$ W m^{-1} K^{-1}, and $g \approx 0.3$ W K^{-1} m^{-1} for CNTs of diameter ~2 nm near breakdown [13]. This gives $R_{Si} = 223.6$ K W^{-1}, $R_{ox} = 4.46 \times 10^3$ K W^{-1}, and $R_C = 462.9$ K W^{-1}, respectively.

We can now calculate the temperature rise at the SiO_2-Si interface, $T_{Si} - T_0 = P_{BD} R_{Si} \approx 1.5$ K near breakdown. This is a good match with the temperature measured by the IR imaging system for this device, considering that most IR signal originates from the top of the heated Si substrate [13-14]. The temperature drop across the SiO_2 is $T_{ox} - T_{Si} = P_{BD} R_{ox} \approx 29.9$ K, and the temperature drop across the CNT-SiO_2 interface is $T_C - T_{ox} = (1 - \gamma_J/2) P_{BD} R_C \approx P_{BD} R_C = 3.1$ K. Thus, the average temperature of the CNN *without* considering the effect of the CNT junctions is merely $T_C \approx 104.5$ °C, much smaller than the breakdown temperature of CNTs in air, $T_{BD} \approx 600$ °C. This remains largely the case even when variability of the CNT-SiO_2 thermal coupling [13] (g) and that of the apparent diameter in SEM $\langle d' \rangle$ are taken into account. In other words,

considering $g = 0.3 \pm 0.2$ W K^{-1} m^{-1} and $30 < \langle d' \rangle < 80$ nm in our analysis leads to a range $T_C \approx$ 90–150 ^{o}C.

We suggest that the "missing" temperature difference is due to highly localized hot spots associated with the CNT junctions, which cannot be directly visualized by the IR thermometry. This is consistent with the emerging picture of CNT junctions being points of high electrical [6-7, 19] and thermal [8-11] resistance. Consequently, we can extract the thermal resistance due to all CNT junctions (R_{JTOT}) in the network acting in parallel

$$R_{JTOT} = \frac{\left(T_{BD} - T_C - T_{ox} - T_{Si}\right)}{\frac{1}{2}\gamma_J P_{BD}} \tag{4.1}$$

The $\frac{1}{2}\gamma_J$ term is the fraction of power dissipated at the junctions, vs. the total power dissipated in the entire network. The R_{JTOT} is bound between 2.1 and 5.9×10^7 K W^{-1} even allowing for variability in the CNT-SiO_2 coupling (g) and $\langle d' \rangle$ as above. This thermal resistance is several orders of magnitude greater than any other thermal resistance in the network.

We now estimate the value of a single CNT-CNT junction with $g \approx 0.3$ W K^{-1} m^{-1} because $R_J \approx R_{JTOT} \cdot (n_J A) \approx 4.4 \times 10^{11}$ K W^{-1}, equivalent to a thermal conductance $G_J \approx 2.27$ pW K^{-1}. Accounting for the variability in CNT-SiO_2 coupling and $\langle d' \rangle$, we estimate R_J to be between 2.7 and 7.6×10^{11} K W^{-1} ($G_J \approx 1.3$–3.6 pW K^{-1}). These values are in good agreement with experimental results obtained for bulk single-wall CNT measurements [9], ~3.3×10^{11} K W^{-1} (3 pW K^{-1}), and one order magnitude greater than values obtained from measurements on intersecting multi-wall CNTs [10]. Our average CNT junction thermal resistance normalized by the average contact area from Figure 4.3 (C), is $r_J \approx 2.1 \times 10^{-6}$ m^2 K W^{-1}. This is one order of magnitude greater than ~10^{-7} m^2 K W^{-1} value predicted by molecular dynamics simulations (MD) for overlapping (10,10) CNTs with 3.4 Å spacing [9, 11], perhaps due to imperfect CNT

junctions in the experiments.

4.4 Discussion and Conclusions

To further understand the large apparent thermal resistance at CNT junctions, we point out this is not only a function of the extremely small overlap area A_J. Considering the strength of the van der Waals (vdW) interaction between two CNTs and between a CNT and SiO_2, we compare the effective spring constants (K) between pairs of atoms. Under the harmonic approximation, $K = \frac{72\varepsilon}{2^{\frac{1}{3}}\sigma^2}$ from a simplified Lennard-Jones (LJ) 6-12 potential [20], where ε is related to the depth of the potential well, and σ is a length parameter. Weighting the effective spring constant for CNT-SiO_2 as $K_{C\text{-}ox} = \frac{1}{3} K_{Si} + \frac{2}{3} K_O$, and using the parameters from [13, 21], we find $K_{C\text{-}ox} > 2K_{C\text{-}C}$. In other words, the CNT-CNT thermal coupling is weaker than the CNT-SiO_2 thermal coupling per pair of atoms interacting through the vdW potential. This simple analysis does not account for the exact shape of the CNTs [13, 21] or the role of SiO_2 surface roughness [13], and thus further work must consider these effects to explain the relatively "high" experimentally observed thermal resistance at single-wall CNT junctions.

In conclusion, we have directly imaged power dissipation in CNN transistors using IR microscopy. We found local hot spots in power dissipation detected by IR correlate to the subsequent breakdown of the network mapped by SEM. Nevertheless, these hot spots do not account for the CNN breakdown at relatively low average temperatures, <150 ^{o}C. Instead, our analysis suggests the CNN breakdown occurs at the highly resistive CNT-CNT junctions, allowing us to extract the junction thermal resistance $R_J \approx 4.4 \times 10^{11}$ K W^{-1} (conductance 2.27 pW K^{-1}). Our findings suggest that transport, dissipation, and reliability of CNN devices is limited by the CNT junctions rather than extrinsic factors such as low substrate thermal conductivity.

4.5 References

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CHAPTER 5

POLYCRYSTALLINE GRAPHENE RIBBONS FOR SENSING APPLICATIONS

Graphene is a 2-dimensional semimetal with zero band gap that exhibits excellent electrical, mechanical, and thermal properties [1-2]. Transport through delocalized pi bonds allows charge carriers in graphene to achieve high mobility[3-4] for both electrons and holes, over ~10^5 $cm^2/V{\cdot}s$ for freely suspended graphene at low temperature and >10^4 $cm^2/V{\cdot}s$ for graphene on SiO_2 [5]. Recent studies have suggested that graphene could also be an interesting chemiresistor material [6-9]. In addition, when functionalized with single-stranded DNA, graphene provides a route towards "sequence-dependent" chemical sensing [10]. Single molecule detection has also been reported [11] using Hall measurements with mechanically exfoliated monolayer graphene. However, prior to this study, the sensitivity of simpler sensing configurations such as two-terminal graphene chemiresistors to many analytes has been below that of chemiresistors based on carbon nanotubes (CNTs) [7-9].

The objective of this work was to understand what limits the sensitivity of simple, two-terminal graphene chemiresistors, and to study these limits in the context of inexpensive devices easily manufactured by chemical vapor deposition (CVD). We focused on the idea that while graphene shares several similarities with CNTs, graphene is a 2-dimensional conductor while CNTs are essentially 1-dimensional conductors. Could this difference in dimensionality be responsible for the difference in sensing behavior?

Further, at this point, the physical mechanisms of interaction between adsorbed species and graphene are not as well understood as in CNT sensors. For instance, we have recently shown that point defects in CNTs are key to the highly sensitive response towards target analytes

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[12-14]. While much of the research within the graphene community is geared towards producing large-scale and defect-free graphene, only recently have linear defects in graphene emerged as a focused area of research [15-17]. The question we then asked is, "Do linear defects enhance the chemical sensitivity in 2-dimensional systems such as graphene?"

5.1 Fabrication of Graphene Sensors

We produced graphene sensors with both nearly-pristine and deliberately-defective structures. Nearly-pristine sensors were obtained by mechanical exfoliation of monocrystalline graphene, while defective graphene was produced by chemical vapor deposition (CVD) of polycrystalline graphene. Both types of graphene sensors were fabricated on SiO_2/Si substrates with metal electrodes defined by standard lithographic techniques.

5.1.1 Fabrication and Characterization of Mechanically Exfoliated Graphene Sensors

Graphene was deposited by mechanical exfoliation from natural graphite with adhesive tape onto a thermally oxidized Si substrate with 100 nm thick SiO_2 [4]. The graphene on substrate was annealed at 400 °C for 35 minutes in Ar/H2 mixture in a furnace to remove glue residue [7]. The number of the graphene layers was confirmed by optical contrast and Raman spectroscopy [1]. In order to define source and drain metal electrodes on the graphene sheet, we deposit 40 nm thick Pd with an adhesive layer of 0.5 nm Cr on the graphene by using electron beam (e-beam) lithography, e-beam evaporation, and lift-off processes. One more e-beam lithography step was used to form a 5 μm wide graphene channel, followed by an oxygen plasma etch. Figures 5.1 (A) and (B) show the optical and atomic force microscopy (AFM) images of a typical exfoliated graphene sensor. Figures 5.1 (C) and (D) show the room temperature resistance vs. gate-to-drain voltage (R-V_{GD}) characteristics for the device in Figure 5.1 (A), and the corresponding resistivity calculated from the measured 4 pt resistance. The red dots indicate

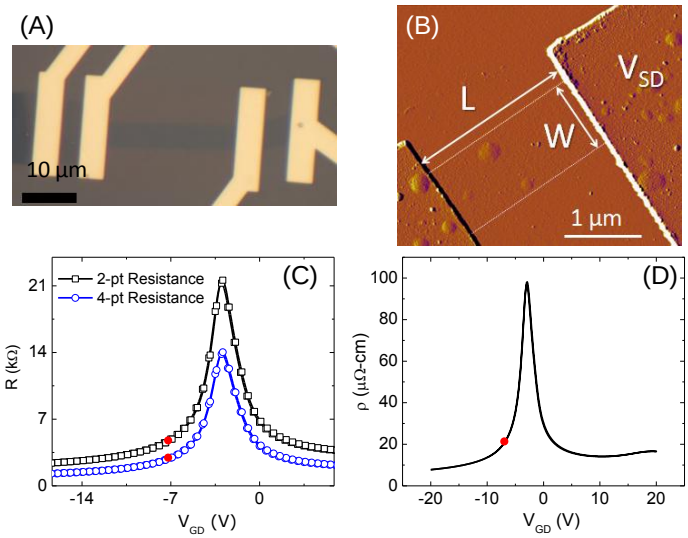

Figure 5.1 Characterization of exfoliated graphene sensors. **(A)** Optical image of the device used in this study. **(B)** Typical AFM phase image of an exfoliated graphene device. **(C)** Room temperature resistance vs. gate voltage (R-V_{GD}) characteristics for the device in (A) (measured in vacuum at ≈ 10^{-5} torr), **(D)** resistivity of the device in (A), calculated from the measured 4 pt resistance. The red dots indicate the corresponding resistance value for the two terminal measurements performed in air prior to chemical sensing measurements.

the corresponding resistance value for the two terminal measurements performed in air prior to chemical sensing measurements.

5.1.2 Fabrication and Characterization of CVD Graphene Sensors

Cr (10 nm)/Au (100 nm) electrodes were first patterned onto Si/SiO_2 substrates using standard lithographic techniques (Figure 5.2 (A)). Graphene films were grown using an Etamota chemical vapor deposition (CVD) system, on 1.4 mil copper foils purchased from Basic Copper (Figure 5.2 (B)). The foils were annealed under Ar/H_2 flow for 45 minutes, and graphene was grown under a CH_4/H_2/Ar flow (17:1:3 ratio) at 1000 °C for 30 min [18]. The resulting Cu/graphene substrates are cooled to room temperature under the same gas flow at a rate of ~20 °C/min. Graphene is subsequently transferred to the sensor electrodes by coating the graphene with polymethylmethacrylate (PMMA), removing the backside graphene in an O_2 plasma, and then etching the backside copper in a 1M $FeCl_3$ solution (Figure 5.2 (C)). Films are rinsed in deionized water (Figure 5.2 (D)) before being "wicked" onto the receiving substrate (Figure 5.2

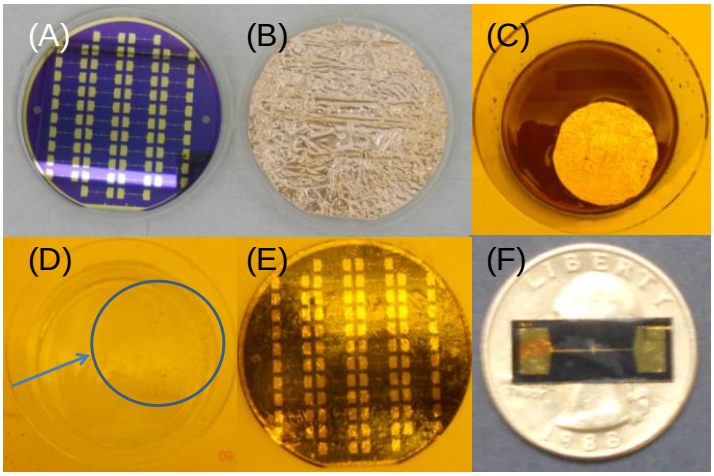

Figure 5.2 Fabrication procedure of wafer scale graphene sensors. **(A)** Cr/Au patterned electrodes. **(B)** 100 mm copper foil with CVD grown graphene. **(C)** PMMA/graphene/copper foil in $FeCl_3$. **(D)** PMMA/graphene in deionized water after etching. **(E)** Sensor electrodes with PMMA/graphene film after transfer. **(F)** Final test structure with transferred and patterned graphene. The sensor electrode dimensions are 1 mm wide by 6 μm long (as drawn).

(E)). PMMA is then removed in a 1:1 solution of methlyene chloride:methanol and sensors are held at 400 ^{o}C for 35 minutes in Ar/H_2 mixture in a CVD furnace to remove residues. While Figure 5.2 illustrates the wafer-scale process of this procedure, we typically process single sensor platforms individually. Extended graphene films, i.e. the graphene covers the entire sensor area (≈6,000 μm^2) and micro-ribbons are defined with standard photolithography using a bilayer of polymethylglutarimide (PMGI) and Shipley 1813 resists. Graphene is patterned by O_2 plasma etching. Photoresist and PMGI are then removed in Remover PG and sensors again held at 400 ^{o}C for 35 minutes in Ar/H_2 mixture in a CVD furnace to remove residues [7, 19]. Figure 5.2 (F) shows the final test structure used for chemical sensing experiments.

To characterize the quality of the graphene films used in this study, Raman spectra were collected using a Renishaw confocal microscope with 633 nm excitation laser and spot size ~1 μm. Spectra are analyzed to quantify graphene layer numbers [18] and estimate crystallite size [20-21]. We then measured the resistance of all of the sensors and selected the ones with low resistance. The measured resistance was between 60 and 70 Ohms for all but one of the samples.

The sheet resistance of the graphene was measured using a HL5500PC Hall effect measurement system in a Van der Pauw configuration. We find the sheet resistance of our ungated (as-deposited) CVD graphene is ~8850 Ω/□. Given the geometry of our sensors (W = 1 mm, L ~ 7 μm), we expect the graphene sensor to have an average channel resistance of ~62 Ω with contact resistance $2R_C < 8\Omega$ (some of which is due to metal leads). Our experiments were designed to compare the response of such graphene chemiresistors made by different procedures, in order to vary the types of defects and determine their role. We note that our four-point measurement showed that contact resistance of our sensors is negligible, indicating negligible role of contacts in the sensing mechanism.

5.2 AFM, Raman Spectroscopy, and X-ray Photoelectron Spectroscopy Characterization

We used AFM, Raman Spectroscopy, and X-ray photoelectron spectroscopy (XPS) to characterize our samples. No evident defects are found in our "pristine" (exfoliated, monocrystalline) samples by AFM or Raman analysis (Figures 5.1 (B) and 5.3 (C)). However, scanning tunneling microscopy (STM) data of similar samples indicate the presence of a few point defects [16]. By contrast, Figures 5.3 (A) and (B) show AFM images of "defective" graphene grown by CVD. The CVD growth process yields polycrystalline graphene, where the grain boundaries can act as linear defects [15, 17, 22]. Transfer processes to remove this polycrystalline graphene from metal growth substrates and place it on insulating substrates also result in wrinkles in the graphene film, which may also act as linear defects [18]. These defects form two different patterns on the graphene surfaces. A few regions of the sample had ~10 μm long well-aligned line defects, like those shown in Figure 5.3 (A). However, the majority of the sample had randomly oriented line defects (Figure 5.3 (B)) with an average length of ~0.7 μm.

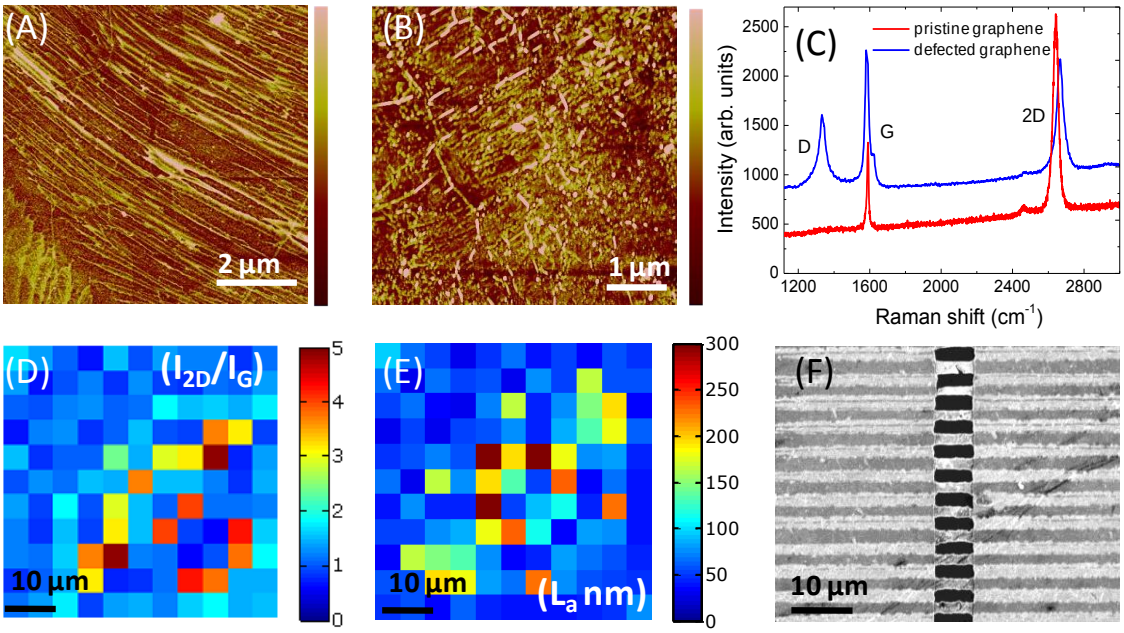

Figure 5.3 (A) and **(B)** AFM images of CVD graphene used for sensors; color scales are 10 and 5 nm, respectively. **(C)** Raman spectra of pristine and CVD-based "defective" graphene samples. **(D)** Map of I_{2D}/I_G ratio indicating our CVD process produces mono to few layer graphene. **(E)** Map of crystallite size indicative of 30 to >300 nm distance between line defects with an average L_a ~ 80 nm (see text). **(F)** SEM image of CVD graphene ribbons.

Raman spectra of both samples are compared in Figure 5.3 (C). The pristine graphene sample does not show a D-peak, suggesting the overall concentration of defects is low and the sample is monocrystalline [23]. By contrast, CVD graphene samples show a large D-peak, from which we can estimate the grain size, L_a (nm) = $2\times10^{-10}\,\lambda^4\left(\frac{I_D}{I_G}\right)^{-1}$, where λ is the excitation laser wavelength and (I_D/I_G) is the D-peak to G-peak integrated intensity ratio [20-21]. We find our CVD sample varies between mono and bilayer graphene (Figure 5.3 (D)), with an average grain size of $L_a \approx 80$ nm (Figure 5.3 (E)). Mobility values for our pristine graphene films are significantly greater than for devices fabricated from CVD graphene (≈3×) (Figure 5.4). We note that with such a small L_a, the Raman spot size of ≈1 µm samples multiple crystallite domains and that the pixel size of the Raman map (5 µm × 5 µm) does not provide any information about the quality of the graphene within a single crystallite. However, this large-scale map provides an

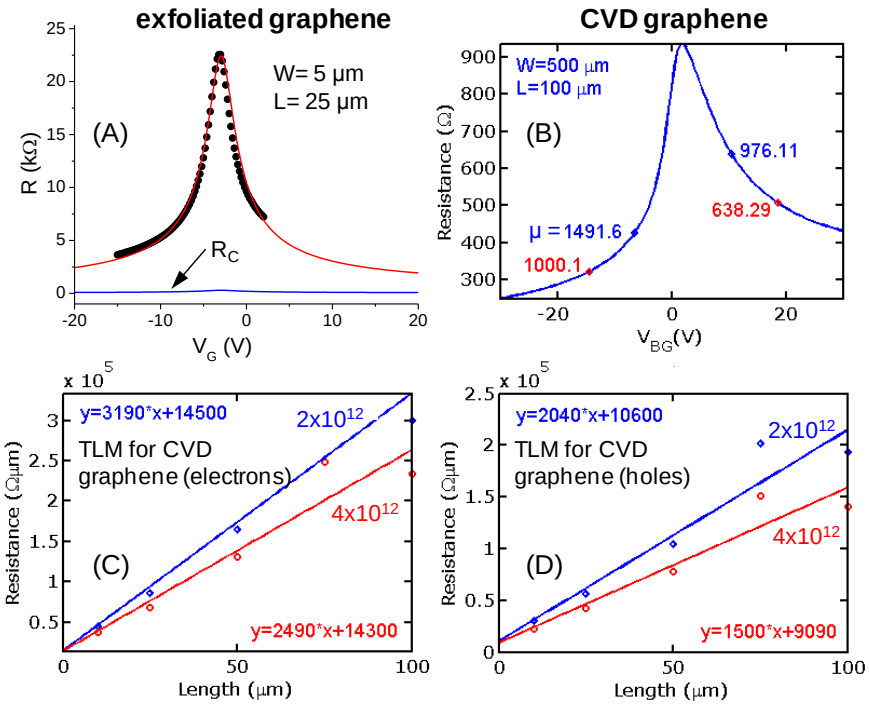

Figure 5.4 (A) *R-V_{GS}* characteristics and curve fitting [24] for exfoliated ("pristine") graphene sample (L = 25 μm, W = 5 μm) with μ ~ 4500 $cm^2/V{\cdot}s$ and R_C ~ 2 kΩ·μm per contact (slightly dependent on gate voltage). Fitting parameters are ρ_c = 500 Ω·μm^2, and n_i=2.8×$^{11}cm^{-2}$. **(B)** CVD-grown graphene (L = 100 μm and W = 500 μm). Best fit mobility indicated on the curve, e.g. μ_p ~ 1000 $cm^2/V{\cdot}s$ at p = 4×10^{12} cm^{-2} hole density, or μ_n ~ 976 $cm^2/V{\cdot}s$ at n = 2 × 10^{12} cm^{-2} electron density. **(C-D)** Transfer length method (TLM) estimate of contact resistance to CVD graphene for samples of varying length. Contact resistance is R_C ~ 7 kΩ·μm for electrons and ~ 5 kΩ·μm for holes, per contact, slightly dependent on gate voltage. The results are consistent with our estimates for CVD graphene in Section 5.1 (e.g. R_C ~ 5-7 Ω for one contact of 1 mm width).

average value of L_a across an area of graphene comparable to the area of the sensors. Scanning tunneling microscopy studies of our CVD graphene reveal the regions between the line defects are almost pristine with large perturbations in the material's electronic properties at linear defects. We have not detected many isolated point defects on our CVD graphene samples [16].

As previously described, we prepared a large-scale CVD graphene film supported by a SiO_2/Si substrate for XPS (Figure 5.5). XPS is accomplished using a KRATOS Axis Ultra 165 mm X-ray photoelectron spectrometer, and conducted at three different locations of our millimeter-scale film. Results indicate our CVD graphene is relatively clean, i.e. there are minimal polymer residues (below the detection limit of XPS) as evidenced by the lack of a peak in the counts per second (CPS) vs. binding energy spectrum near the C-1S peak at ≈ 290 eV [25].

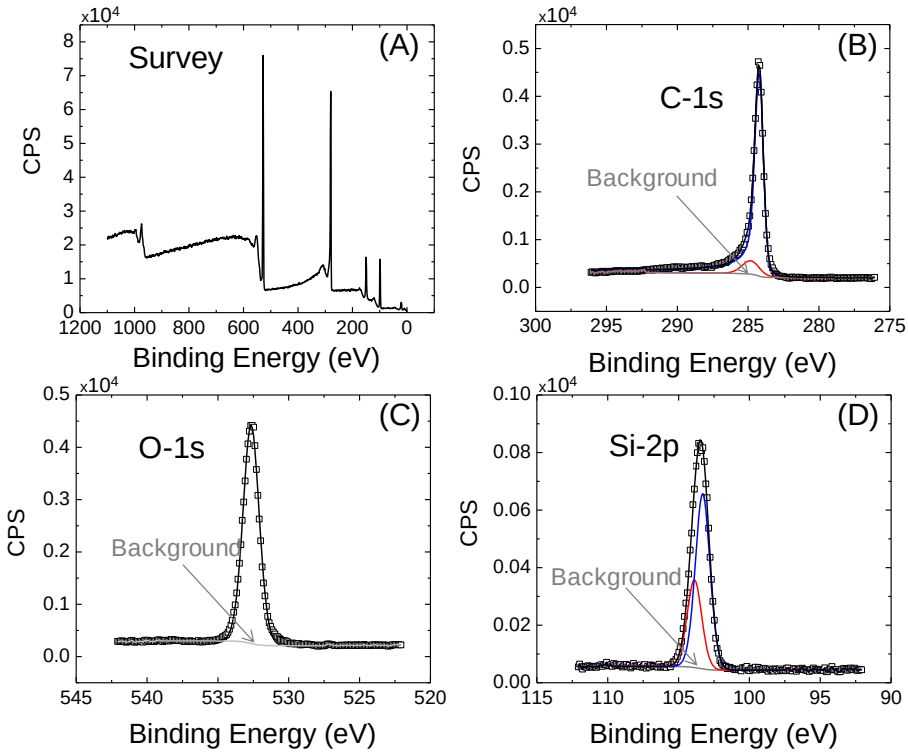

Figure 5.5 Typical XPS results of counts per second (CPS) vs. binding energy for our graphene samples grown via CVD and transferred to SiO_2/Si substrates. **(A)** XPS survey. **(B)** C-1s peak. **(C)** O-1s peak. **(D)** Si-2p peak. The lack of a peak at ≈290 eV is indicative of the lack of PMMA residues in our samples after processing [25]. In (B-D) open squares are raw data and solid lines are fits.

We also do not see evidence of a C-O bond in the C-1s peak. This result is confirmed by the lack of peaks above the adventitious hydrocarbon peak at 284.6 eV, and by the single O-1s peak near 582 eV [25]. The intensity of the graphene peak was determined by fitting the C-1s region collected at an electron emission angle of 0° using a Shirley background and a Doniach-Sunjic line-shape for graphene based upon fitting the C-1s of highly ordered pyrolytic graphite [26].

5.3 Chemical Sensing Methods

Sensors were placed in a custom-built polyaryletheretherketone (PEEK) flow cell, and a fused silica passivated capillary was used to connect to a gas chromatograph (GC) inlet. An Agilent 6893N GC/FID-MS with 7683B auto-sampler with a pulse of 100 ms was used to deliver target gas molecules to the sensors at pressure of 3.6 psi for all experiments. Ultra pure helium

was used as a carrier gas at fixed flow rate. A VoltaLab 10 potentiostat (PGZ100) was used to monitor the change in potential on the sensors upon exposure to trace gas vapors [27]. The sensors were exposed to 100 milliseconds of toluene (an electron donor) and to 1,2-dichlorobenzene (an electron acceptor), and the change in the conductance was measured upon exposure to trace gas vapors.

5.4 Chemical Sensing Properties of Graphene Chemiresistors

Figures 5.6 (A) and (B) compare the response of the two different chemiresistors to a 100

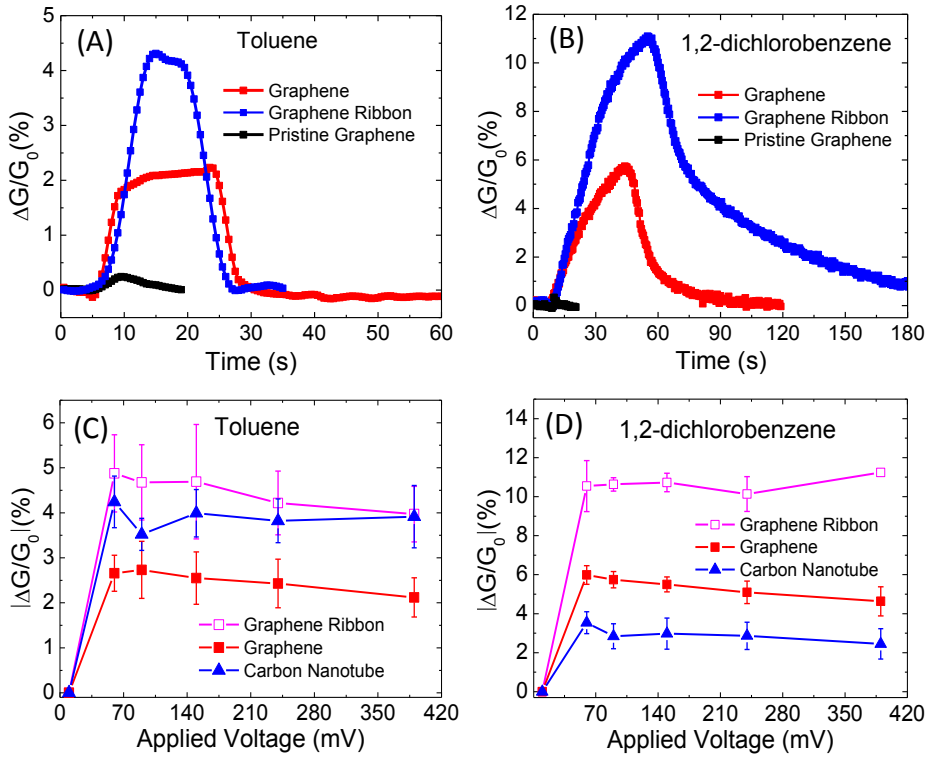

Figure 5.6 (A-B) Ratio of conductance to initial conductance (G/G0) response of CVD-grown defective graphene, CVD graphene microribbon, and 5 μm wide pristine (exfoliated) graphene sensors to 10^{14} molecules of toluene and 10^{15} molecules of 1,2-dichlorobenzene, respectively. The pulses are similar to those produced by a preconcentrator [28] sampling air containing 300 ppb of analyte. **(C-D)** Expanded response as a function of applied voltage. It is seen that the sensors do not show a detectable response at low voltage, but turn on when the applied voltage exceeds 50 mV. Details of the jump in sensitivity have been described previously [29]. The CVD graphene microribbon sensors show the response to 1,2-dichlorobenzene is 3 to 4 times higher than that of CNT sensors and 2 times higher than that of CVD graphene sensors. The CVD graphene microribbon sensors also show higher response to toluene molecules compared to CNT based and CVD graphene sensors.

millisecond pulse of toluene (an electron donor) and to 1,2-dichlorobenzene (an electron acceptor). In each case, we chose the number of molecules in the pulse to be similar to the number of molecules produced by our preconcentrator [28] with sampling air containing 300 parts per billion (ppb) of analyte. We find little or no response with the pristine graphene sample, but a large response (up to 50× higher) with the defective and polycrystalline samples. Clearly, the addition of line defects (and perhaps a few point defects) has enhanced the sensor response. We note that we have used well-established cleaning procedures to eliminate PMMA residues left after the graphene device fabrication for both types of samples, and X-ray photoelectron spectroscopy (XPS) verifies our cleaning procedure removes PMMA as previously described [7, 19].

We performed an additional experiment to further elucidate the role of line defects on the behavior of our sensors. In this case, we cut the CVD-grown sample into ribbons that were 2 to 5 μm wide, as shown in Figure 5.3 (F). By way of background, when a graphene sheet is cut into ribbons with dimensions similar to those of the line defects, edges are created that cross the line defects. Consequently, when an edge crosses a line defect, leakage currents around the sides of the line defect are eliminated. Thus, the edge should enhance the effects of the line defects, provided the length of the line defects is similar to the ribbon width. Point defects should be hardly affected since most of the point defects are far away from the edges.

The edges themselves do not affect charge transport significantly, so edges alone should have very limited effect on the sensor response; this is the case here because the charge carrier mean free paths are of the order ~20 nm while the ribbons are 2 to 5 μm wide. The carrier mean free path, l can be calculated estimated by using a semiclassical relation between the mobility

and the mean free path [30], $l = \left(\frac{h}{2q}\right)\mu_0\left(\frac{n}{\pi}\right)^{\frac{1}{2}} \approx 16$ nm, for $n = 2 \times 10^{12}$ cm^{-2} and $\mu_0 = 1000$ cm^{2}V^{-1}s^{-1} for the CVD grown graphene FET. Here, h is the Planck constant and q is elementary charge. In addition, for the exfoliated graphene, $l \approx 74$ nm for $n = 2 \times 10^{12}$ cm^{-2} and $\mu_0 = 4500$ cm^{2}V^{-1}s^{-1}. Therefore, after scattering by an edge of our wide graphene channel (2~5 μm wide), it is highly probable the carriers experience numerous scattering events in the inner region of the ribbon before the next edge scattering event occurs. Consequently, we can neglect the conductance change due to the adsorbed molecules at the edges of the graphene channel.

Our pristine (monocrystalline) graphene ribbon chemiresistor had a width of 5 μm. We observe a negligible sensor response, showing that the combination of narrowly spaced edges and a few point defects is insufficient to cause a significant change in the conductance under sensing conditions. In contrast, when the defective (CVD-grown) graphene sensors with existing line defects are cut into microribbons, the chemiresistor response further increases by a factor of 2 to 4 compared to unpatterned CVD-grown graphene chemiresistors, as shown in Figures 5.6 (A) and (B). The sensitivity is enhanced into the parts per billion (ppb) range. Clearly, the combination of edges and line defects enhances the response of the sensor, compared to edges or line defects alone. Further, this experiment proves that in our samples the line defects have a large effect on the response because cutting the graphene into ribbons should only affect the line defects and not the point defects.

Figures 5.6 (C) and (D) also compare the response of the graphene ribbon chemiresistors to CNT-based chemiresistors. In each case we plot the average response of five different sensors. Notice that the sensor response exceeds that of CNT chemiresistors, suggesting that graphene

sensors with edges and line defects offer larger sensitivity to analytes than do CNT sensors with point defects alone.

5.5 Simulation of Graphene Chemiresistors

In order to understand the experimental observations described above, we performed calculations of conduction in graphene chemiresistors with and without the presence of line defects and analytes. We used COMSOL Multiphysics to build a 2-dimensional finite element model seeking to understand how electric fields change near point and line defects. The modeled graphene chemiresistors have dimensions of $5 \times 5\ \mu m^2$ and $1 \times 5\ \mu m^2$ (for the ribbon device), with a resistivity of $2.1 \times 10^{-5}\ \Omega \cdot cm$ as measured in our exfoliated graphene sensors. A fixed potential (0.1 V) is applied to the left boundary of the chemiresistor while plotting out the steady state electric field distribution.

Figure 5.7 (A) shows the distribution of the electric field in a graphene sheet with one hundred 30 nm wide islands containing analytes, as a model for point defects. We assumed the analyte would increase the local resistance of the graphene by 100 times (i.e. significantly more than that one might expect), and did calculations to determine whether there was a significant change in the resistance of the overall device. For the non-defective graphene we used the measured resistivity of our exfoliated graphene, $2.1 \times 10^{-5}\ \Omega$ cm. Surprisingly, there was very little effect from point defects. The electric field lines around the point-like defects did not change notably, and there was little change in the overall resistance of the device.

Physically, electrons take the path of lowest resistance in carbon devices [14], as in other materials. An isolated point defect or other localized chemisorption site does not lead to a significant change in the resistance of the chemiresistor because there is still a low-resistance pathway for electron conduction in analyte-free regions of the graphene. In effect, the low-

resistance pathways short-circuit the analyte. As a result, according to our calculations, a localized change in the graphene resistance due to adsorption of an analyte will not have a significant effect on the chemiresistor response unless the analyte concentration is very high. This explains why pristine graphene (i.e. monocrystalline and without defects) is less sensitive to analytes.

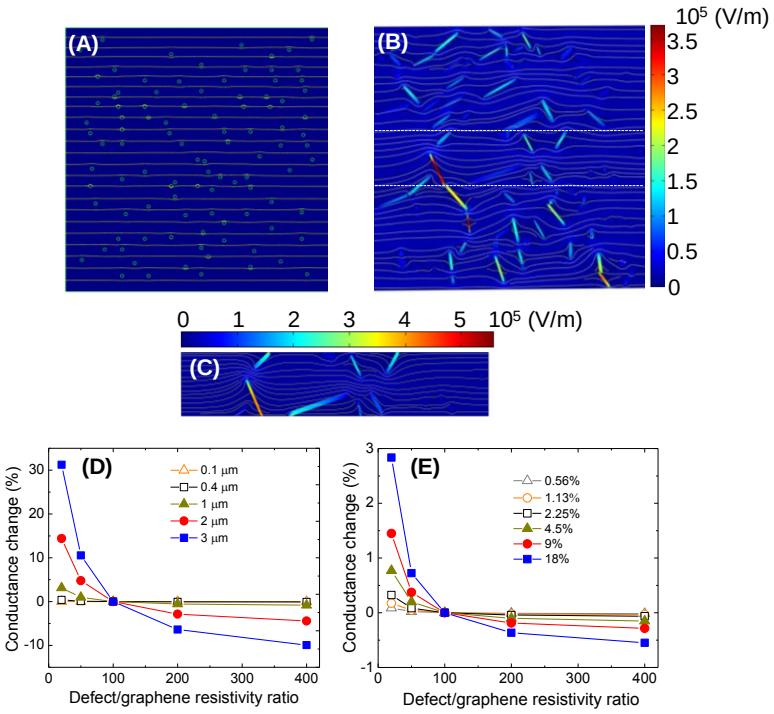

Figure 5.7 (A) Finite-element simulation of electric field distribution in a 5 × 5 μm^2 graphene sample with 100 point defects of 30 nm size. **(B)** Electric field distribution in a 5 × 5 μm^2 graphene sample with line defects which mimic the topography measurement by AFM of an actual graphene sensor shown in Figure 5.1 (B). **(C)** A 1 × 5 μm^2 graphene ribbon with randomly distributed line defects. This graphene ribbon is the portion of the sample between the dotted lines in (B). The graphene resistivity is 2.1×10^{-5} Ω·cm and defect resistivity is 100 times higher. The color bar shows the electric field strength (max: 3.7×10^5 V/m), whereas the streamlines indicate the current density. **(D-E)** Show the numerical modulation of the chemiresistor conductance when the resistivity ratio of defects to pristine graphene changes from 20×, 50×, 100×, 200× and 400×. The baseline conductance is chosen at 100×. In (D), the line defect widths are constant at 0.1μm and the lengths were increased from 0.1 to 3 μm (0.12% to 3.6% of the area). In (E), the point defect concentration (per area) increased from 0.56%, 1.1%, 2.2%, 4.5%, 9%, and 18%. We clearly observed that even at relatively high concentration, the effect of point defects on the conductance change (%) is very small (only 3% change for 18% of defect concentration), while the effect of line defects is significant (32% change for 3 μm defect length, 3.6% of area).

On the other hand, line defects such as those observed by previous investigators [15, 31-33] could have a much stronger effect on the resistance of graphene. Figure 5.7 (B) shows a simulation of the effect of line defects on the current flow through the chemiresistor. The defect geometry is similar to that observed by AFM (Figure 5.3 (B)). Notice that, according to the calculations, the presence of line defects or a closely spaced line of point defects greatly perturbs the electric fields and conduction through the chemiresistor. Line defects are needed because graphene is a 2-dimensional conductor. In such a case, the pathways around the line defects are long enough to be difficult to short-circuit. The effects of line defects are more pronounced in a graphene ribbon sample (Figure 5.7 (C)), when the lengths of the line defects are comparable to the sample width. One would expect the adsorption of chemical vapors on low-energy sorption sites of line defects to have an important effect on the resistance of the chemiresistor. In a previous work [34], we found that concentration of analytes tested here was about 6000 times higher on point defects than on the pristine region of carbon nanotubes. We would expect a similar concentration enhancement on line defects. This high concentration of adsorbed molecules can induce large interactions locally [35]. While our Raman analysis indicates our CVD growth of graphene results in a large percentage of bilayer regions, ($2 > I_{2D}/I_G > 1$) [36], the change of the conductance originated by the electric field from adsorbed molecules will affect the sensitivity of both monolayer and bilayer films because the screening length perpendicular to the graphene plane is greater than the monolayer thickness, or about 0.6 nm [37]. The results in Figures 5.7 (A) and (B) provide the basis for our understanding of the graphene chemiresistor response.

We used a simplified model with well-aligned linear defects to explore the effects of defect geometry on the sensitivity of the chemiresistors. Our numerical technique is to vary the

resistivity ratio between defects to pristine graphene, indicative of the modulation of defect sites upon exposure to analyte molecules. We then measure the change in conductance (%) and choose the baseline conductance at 100×. Point defects are randomly distributed to account for 0.6% to 18% of the graphene area. We also changed the length of the line defects from 0.1 to 3 μm, 0.12% and 3.6% of the graphene area, respectively. In Figure 5.7 (D) and (E), we plotted how the conductance of the chemiresistor changes when the resistivity ratio between defects to graphene changes from 20× to 400×, for every geometry. Results clearly indicate that the conductance of graphene is more sensitive to the geometry of the defects rather than their concentration.

According to this simple model, pristine graphene or graphene with low concentrations of randomly distributed point defects are less sensitive to the adsorption of gas, because adsorbed molecules on point defects are easily short circuited given the 2-dimensional nature of current flow in graphene. In contrast, line defects are more effective in promoting chemiresistor response. We note a more rigorous modeling approach would self consistently take into account the carrier concentrations, potential (field) profile, and band structure modification by adsorbates [38]. However, we believe that the simple model presented here contains the more salient features of the physical response. Future work with three-terminal chemFETs will also allow for more detailed modeling and a better understanding of the carrier density distributions controlled by the gate terminal.

5.6 Conclusions

Our results suggest that the response of graphene chemiresistors depends on the types and geometry of their defects. Nearly-pristine graphene chemiresistors are less sensitive to analyte molecules because adsorbates bind to point defects [31], which have low-resistance pathways

around them. As a result, adsorption at point defects only has a small effect on the overall resistance of the device. On the other hand, micron-sized line defects or continuous lines of point defects are different because no easy conduction paths exist around such defects, so the resistance change after adsorption is significant. We also conclude that the 2-dimensional nature of defective, CVD-grown graphene chemiresistors causes them to behave differently than CNT chemiresistors. Moreover, this sensitivity is further improved by cutting the graphene into ribbons of width comparable to the line defect dimensions (microns in this study). Thus, graphene ribbons with line defects appear to offer superior performance as graphene sensors. Future work to engineer line defects and edges could further enhance the graphene chemiresistor sensitivity.

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CHAPTER 6

THERMAL TRANSPORT IN LAYER-BY-LAYER ASSEMBLED POLYCRYSTALLINE GRAPHENE VAN DER WAALS SOLIDS

As we near the tenth anniversary of the discovery of the electric field effect in graphene [1], the emerging applications of this atomically thin material validate the enormous research efforts put forth to understand its physical properties and large-scale synthesis. Graphene has generated such interest due to its exceptional intrinsic properties. For example, the room temperature thermal conductivity (κ) of graphene is the highest of any material ever measured, $\kappa \approx$ 2,000 to 4,000 $Wm^{-1}K^{-1}$ [2-3]. Furthermore, graphene's intrinsic carrier mobility exceeds 100,000 $cm^2/V \cdot s$ [4], it has a Young's modulus of ≈1TPa [5], a high optical transparency of ≈98% [6], and a high specific surface area of ≈2600 m^2/g [7]. Graphene can also carry large electrical [8] and electrochemical [9] current densities, $\approx 2\times10^9$ and 1.2×10^4 A/cm^2, respectively. These properties have facilitated a wide range of applications, such as transparent and flexible electrodes [10-11], nanoscale interconnects [8, 12], chemical sensors [13-16], mechanical resonators [17], transistors [18-20], lithium-ion batteries [21], biological sensors [9, 22-24], and integrated circuits [25-26].

The applications of graphene, however, depend largely on the quality of the material and its related production costs [27]. Large-scale methods of graphene production, such as liquid exfoliation of graphite [28] and chemical vapor deposition (CVD) on transition metal substrates [29-30], can result in a large amount of defects. Such defects may be beneficial for applications such as chemical sensors [15, 31], but detrimental to electrical [32-36] and thermal [37-39] transport for applications in transistors or as thermal heat spreaders. Sublimation of Si from SiC wafers [40] provides high-quality graphene, but is more expensive than CVD growth, which provides similar quality graphene if grown on the correct metal surface under optimized conditions [36,

41]. Mechanical exfoliation of graphene from bulk graphite also provides high-quality graphene crystals, but is limited to producing prototype devices in research environments [1, 27].

More recently, graphene is being combined with other 2-dimensional crystals, such as hexagonal boron nitride and MoS_2, to form multilayer structures. These layer-by-layer (LBL) assembled materials lead to artificially stacked van der Waals (vdW) solids for new device applications [42-44]. VdW solids have strong in-plane bonds and weak inter-layer vdW interactions (like natural graphite); however, LBL assembly could lead to tunable and highly anisotropic heat transport properties between the in-plane and cross-plane directions [45-46]. Therefore, LBL assembled films constructed from large-scale polycrystalline graphene grown by CVD present an interesting material systems to investigate the role of external influences on thermal transport, (e.g. defects and substrates) on the thermal properties of vdW solids.

6.1 Thermal Conductivity of Graphene

Table 6.1 summarizes selected graphene κ data from the literature to highlight the role of the substrate and number of layers on thermal transport in graphene. The κ data for bulk single crystal diamond, the in-plane thermal conductivity ($\kappa||$) of graphite, and the cross-plane thermal conductivity ($\kappa\perp$) of graphite [47] are included for comparison. The $\kappa||$ for freely suspended graphene ranges from about 2000 to 4000 $Wm^{-1}K^{-1}$ [3]. By comparison, the room temperature κ of diamond is ≈2200 $Wm^{-1}K^{-1}$ and the $\kappa||$ of graphite is ≈1950 $Wm^{-1}K^{-1}$ [47]. At the other end of the carbon materials κ spectrum, the room temperature $\kappa\perp$ of graphite is ≈6 $Wm^{-1}K^{-1}$, limited by weak vdW interactions between adjacent layers [47]. Thermal transport perpendicular to graphene and few-layer graphene (FLG) is also limited by weak vdW interactions with the adjacent substrates or layers [48-49].

Table 6.1 Selected thermal conductivity values from the literature

Material	κ ($Wm^{-1}K^{-1}$)	Method	Refs.
Highly Ordered Pyrolytic Graphite [a](||), [b](⊥)	~ 2000[a] ~6[b]	Various	[47]
Exfoliated Graphene (Suspended) $(\|\|)$	~ 3,000 – 5,000	Raman Optothermal	[50-51]
Exfoliated Graphene (Supported) $(\|\|)$	~600	Electrical Thermometry	[52]
Exfoliated Few Layer Graphene, n=5[a], 4-2[b] (Suspended) $(\|\|)$	~170[a] ~ 1,300 – 2,800[b]	[a]Electrical Thermometry [b]Raman Optothermal	[53-54]
Exfoliated Few Layer Graphene, n=3, L=1, 2, 5 μm (Supported) $(\|\|)$	~150–1250	Electrical Thermometry	[53]
CVD Graphene (Suspended) $(\|\|)$	~2,500	Raman Optothermal	[55]
CVD Graphene (Au/SiN Supported) $(\|\|)$	~ 50–1020	Raman Optothermal	[55]

The role of a substrate on thermal transport in supported graphene was first reported by Seol et al., and further substantiated by the Raman thermometry measurements of Cai et al. a short time later [52, 55]. The room temperature $\kappa||$ of substrate supported graphene was found to be ≈600 $Wm^{-1}K^{-1}$ for mechanically exfoliated graphene on SiO_2, and between ≈50 and 1020 $Wm^{-1}K^{-1}$ for graphene grown by chemical vapor deposition and in contact with gold coated silicon nitride. Jang *et al.* later reported a further reduction in the room temperature κ of mechanically exfoliated graphene which was encased in 30 nm of e-beam evaporated SiO_2 ($\kappa||$ ≈160 $Wm^{-1}K^{-1}$), but which recovered the $\kappa||$ of graphite after about 20 layers [56]. Lastly, electrical thermometry measurements performed by Wang et al. show that the $\kappa||$ of FLG (n = 3) nearly recovers that of bulk graphite (κ_{FLG} ≈1250 $Wm^{-1}K^{-1}$) when thermal transport in the sample is diffusive [53]. Allowing for differences in the quality of the graphene samples, the reduced κ values for substrate supported graphene and encased graphene are still in stark contrast to that of freely

suspended graphene. These decreases in intrinsic thermal conductivity of "bulk" graphene can be attributed to scattering of graphene phonons by the substrate phonons [52, 57]. Combined, these results suggest substrate phonons have an associated length scale over which they can scatter phonons in adjacent 2-dimensional crystals. Moreover, they highlight the possibility of tuning the thermal anisotropy in vdW solids composed of randomly stacked 2-dimensional crystals, which has not yet been experimentally demonstrated. Additionally, it is interesting to note that the $\kappa||$ of substrate supported polycrystalline graphene has not been fully elucidated over a wide temperature range, which has important technological implications for thermal heat spreading and interconnect applications because additional phonon scattering due to grain boundaries is likely to further reduce the κ as compared to substrate phonons alone [38, 52, 57].

A simple yet versatile approach to measuring thermal properties at the nanoscale is by steady state electrical thermometry. This method induces a temperature rise on one side of the sample by flowing current through a metallic heater, generating Joule heating. Temperature gradients across the sample are sensed by measuring calibrated changes in the resistance of a nearby metallic sensor. For example, electrical thermometry has been used to measure the κ of ultra-thin (<500 nm) and freely suspended bismuth films, illustrating how the combination of this technique with confined heat flow results in highly sensitive κ measurements [58]. More recently, advances in microfabrication technology have enabled the use of even thinner suspended membranes and steady state electrical thermometry to measure the lateral κ of various thin films, thin film stacks, and nanostructures. Typically, these suspended thermal test structures use SiN membranes because of the robustness of the suspended film even at ~100 nm thickness. This robustness is attributed to the membrane's high tensile strength, which allows it to be "stretched" over trenches etched into the supporting Si substrate [59-63]. However, such platforms are often diffi-

cult to fabricate, resulting in low yield. Additionally, not all membrane suspension processes are compatible with a wide range of nanomaterials.

In this study, we develop a suspended electrical thermometry platform, fabrication process, and measurement technique which are compatible with a wide range of nanomaterials and offer ≈10 mK temperature resolution in order to explore the thermal coupling between graphene based vdW solids and their dielectric environment. Experimentally, polycrystalline graphene is grown on copper foils purchased from Alfa Aesar (CAS 7440-50-8), and then transferred through a wet-transfer process using polymer supports [9, 11, 15, 30]. Metal heater and sensor strips are patterned on top, and the wafer is back-etched to suspend the supporting dielectric membrane (Figure 6.1). A heating current (~50 to 350 μA) is passed through the middle electrode, while the temperature is sensed by monitoring calibrated changes in the electrical resistance of the two sensors. One side of the measurement platform provides the thermal conductance (G_{TH}) of the graphene and substrate, while the other measures only the supporting dielectric film. The effective G_{TH} of the graphene (LBL graphene stack) sample is thus obtained by subtraction. Comparison of a single transferred layer of CVD graphene to LBL assembled stacks of CVD graphene, as well as to nonequilibrium Green's functions, is done to elucidate the role of the supporting substrate and graphene grain boundaries on the film's thermal properties.

6.2 Suspended Thermometry Platform Fabrication Process

Step 1 – Wafer preparation, etch stop layer, and low stress SiN deposition: 275 ± 25 μm Si wafers were cleaned in a Piranha solution (5:1 H_2O_2 to H_2SO_4) at 120 °C for 15 minutes followed by a 5 minute rinse in deionized water. The wafers were then dried under an N_2 flow and the native oxide etched in a 10:1 buffered oxide etch (BOE) prior to atomic layer deposition (ALD) of a thin Al_2O_3 etch stop layer. Then 20 nm of Al_2O_3 were deposited using a Cambridge

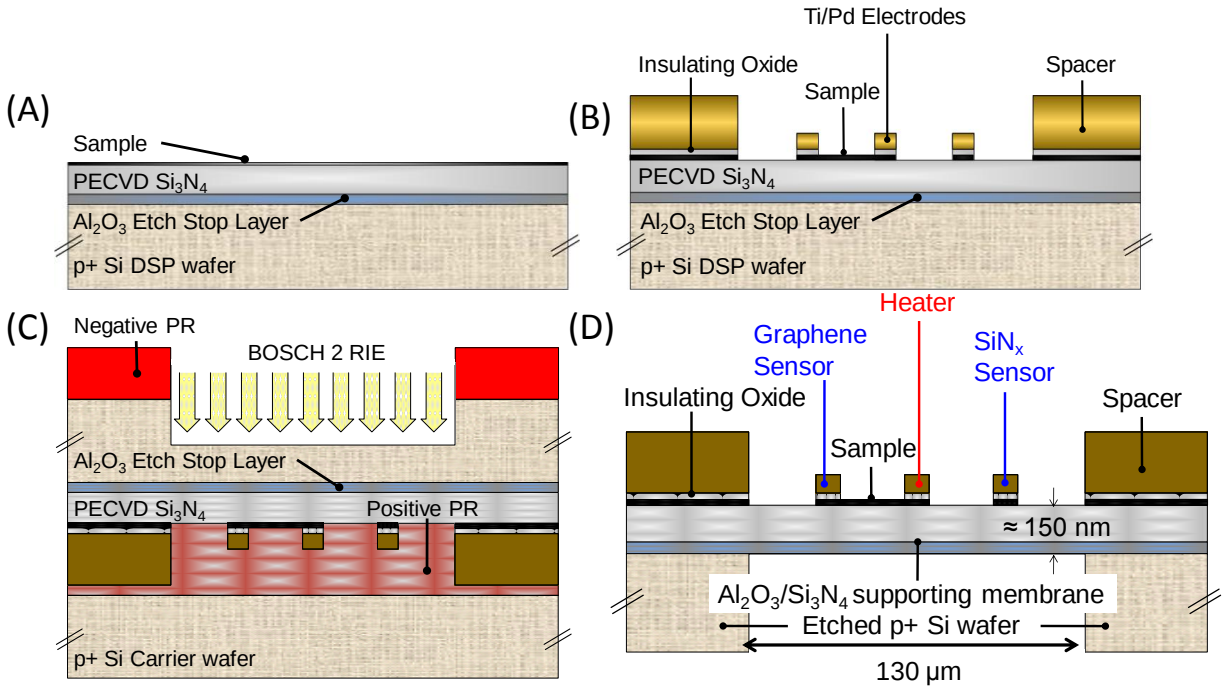

Figure 6.1 Suspended electrical thermometry platform fabrication process. **(A)** Al_2O_3, PECVD SiN, and the graphene sample are deposited on a dual-side polished Si wafer. **(B)** Electrodes, spacers, and graphene samples are patterned with standard photolithographic techniques. **(C)** Backside features are aligned to topside features and the sample is mounted to a carrier wafer for through wafer etching with a BOSCH 2 reactive ion etching (RIE) process. **(D)** Final schematic of suspended thermometry platform. The insulating oxide prevents electrically conducting samples (e.g. graphene) from shorting the heater and sensor. The spacer adds a gap between the suspended membrane and the carrier wafer during the release step.

Nanotech ALD system. The silicon wafer was heated to 250 °C in the reaction chamber, and trimethyl aluminum (TMA) and water vapor were pulsed into the chamber to deposit Al_2O_3 with atomic layer precision. Next, approximately 150 nm of SiN was deposited using a STS Multiplex CVD system in a mixed frequency mode (Figure 6.1 (A)).

Step 2 – Graphene growth and transfer: We grow graphene using a low-pressure chemical vapor deposition (LPCVD) system on 1.4 mil copper foils purchased from Alfa Aesar (CAS 7440-50-8). We anneal the copper foils at 1000 °C under Ar/H_2 flow for 60 minutes, at a base pressure of ≈4.5 torr. Graphene is grown for 20 minutes at 1000 °C under CH_4 and H_2 flows at ≈0.5 torr. The resulting graphene and copper substrates are cooled to 150 °C under the same CH_4 and H_2 flow at a rate of ≈10 °C /minute, followed by cooling to room temperature under Ar flow.

We coat one side of the Cu foil with a bilayer of PMMA (495K and 950K). We etch the backside graphene for 30 seconds in O_2 plasma and the copper foil in Transcene CE-100 overnight. The resultant PMMA/graphene film is rinsed in a series of dilute HCl and deionized water baths before being wicked onto the receiving substrates, prepared as described in Step 1 (Figure 6.1 (A)). PMMA is removed in a 1:1 methylene chloride/methanol solution for 30 minutes followed by a 400 °C anneal under Ar and H_2 flow. The transfer process is repeated when building LBL assembled graphene stacks.

Step 3 – Lithographic patterning and electrode deposition: The heater and sensor electrodes are patterned using standard lithographic techniques. A thin layer of polydimethylglutarimide (PMGI-SF5) lift-off resist was spun onto the graphene/SiN samples at 3000 RPM for 30 seconds, followed by a 5 minute bake at 150 °C. The sample is then coated with ≈1.5 μm of Shipley 1813 photoresist and baked at 110 °C for 75 seconds. Exposure is done through a dark field mask (≈ 40 mJ/cm^2), and the patterns are developed using MF 319 developer. The sample is then placed in electron-beam evaporators for deposition of 20 nm of SiO_2, 5 nm titanium (Ti), and 30 nm of palladium (Pd). Evaporators are evacuated to a base pressure of 8×10^{-7} torr before deposition. Liftoff is performed by placing the sample in Remover PG at 80 °C. Similar lithographic processes are performed to pattern the between the center and an edge electrodes, as well as to increase the metal thickness of the metal pads to 100 nm. Graphene patterning is performed by O_2 plasma etching for 45 seconds at 100 watts at a background pressure of 100 millitorr (Figure 6.1 (B)). The extra thickness of the metal pads aids in wirebonding, but also serves as a spacer for the device active region during backside processing. Importantly, the graphene must be removed from underneath the metal pads in order to perform the wirebonding needed for thermometry measurments.

Step 4 – Backside patterning and membrane suspension: Prior to backside processing, the topside structures of the wafer can be protected by applying a bilayer of PMGI-SF5 and S1813 photoresist as previously described. The PMGI underlayer is essential to prevent the "hard baking" of the S1813 photoresist from contaminating the topside features. The back side of the sample is patterned by spin coating NR5-8000 at 3000 RPM for 40 seconds (≈ 8 to 9 μm). The photoresist is baked at 150 °C for 60 seconds. Alignment to topside features is done using a Quintel UL 7000 series mask aligner with an infrared (IR) through wafer backside alignment tool. Exposure is performed through brightfield mask (≈25 mJ/cm^2). The sample is then baked at 100 °C for 60 seconds and backside patterns are developed using RD6 developer. The wafer is attached to a carrier wafer for backside etching in an anisotropic deep silicon etching system. A BOSCH 2 process is used to etch completely through the wafer (Figure 6.1 (C)). The high selectivity of the BOSCH 2 process to Si over Al_2O_3 facillitates increased yield in the process [64]. The Al_2O_3 prevents any etching of the thin SiN membrane, which could occur due to variance in the wafer thickness or nonuniform etch rates across the platen area of the deep silicon etching system. After verifying through wafer etching by optical microscopy, the carrier wafer and samples are immersed in Remover PG, releasing the sample and suspending the thermometry platform membrane.

6.3 Materials Characterization

Raman mapping of graphene was performed using a scanning confocal Renishaw Raman microsope (inVia and WiRE 3.2 software). Data were collected using a 633 nm edge emitting laser (laser spot size ≈ 1.3 μm and ≈ 0.1 mW incident power), a 50× long working distance objective, a 1800 lines/mm grating, and 30 second acquisition time. 121 spectra were collected over a 20 μm × 20 μm area at a 2 μm step size and analyzed by fitting mixed Gaussian and Lorentzian

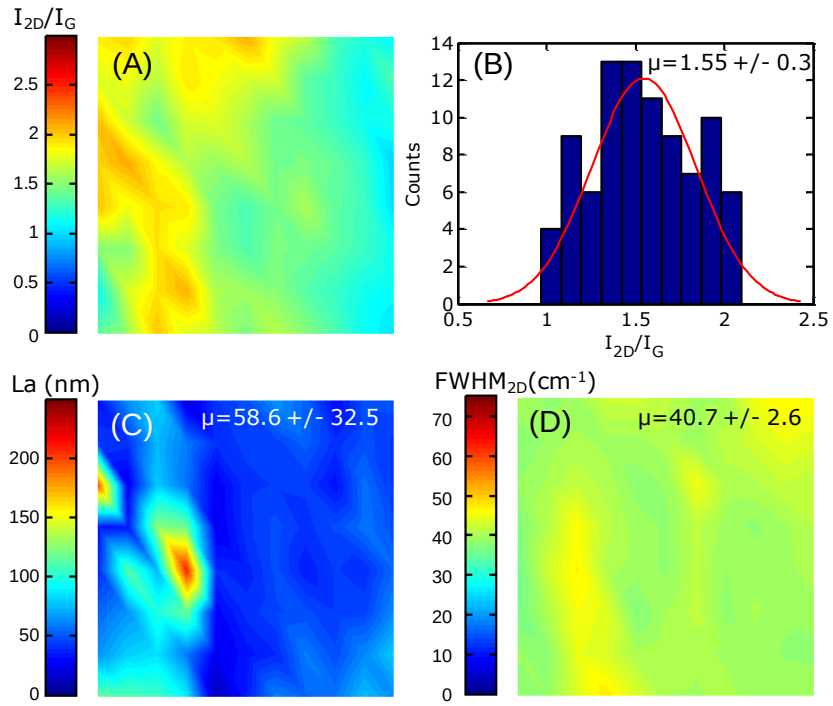

Figure 6.2 Raman analysis of a single transfer of CVD graphene. **(A)** I_{2D}/I_G ratio indicating predominantly monolayer coverage. **(B)** Histogram of data in (A), with mean and standard deviation as indicated. **(C)** Graphene crystallite size (La) extracted data shown in Figure 6.3. **(D)** FWHM of the 2D peak suggesting the CVD graphene is predominantly monolayer with some bilayer regions.

curves around the D, G, and 2D Raman peaks centered at ≈1340, 1590, and 2660 cm^{-1}, respectively. A cubic spline interpolation was used to subtract the background before curve fitting. The Raman spectroscopy maps of the graphene 2D to G-peak intensity ratios (I_{2D}/I_G) (Figures 6.2 (A) and (B)) and the full-width at half-maximum of the 2D peak ($FWHM_{2D}$) (Figure 6.2 (D)) show our growth process results in predominately monolayer graphene. Our CVD graphene samples are polycrystalline, and exhibit a D-peak in the Raman spectra from which we can estimate the grain size, L_a (nm) = $2\times10^{-10}\,\lambda^4\left(\frac{I_D}{I_G}\right)^{-1}$, where λ is the excitation laser wavelength and (I_D/I_G) (Figures 6.3 (A) and (B)) is the D-peak to G-peak integrated intensity ratio [65-66]. We find our CVD graphene has an average grain size of L_a ~ 58.6 ± 32.5 nm (Figure 6.2 (C)), which is in

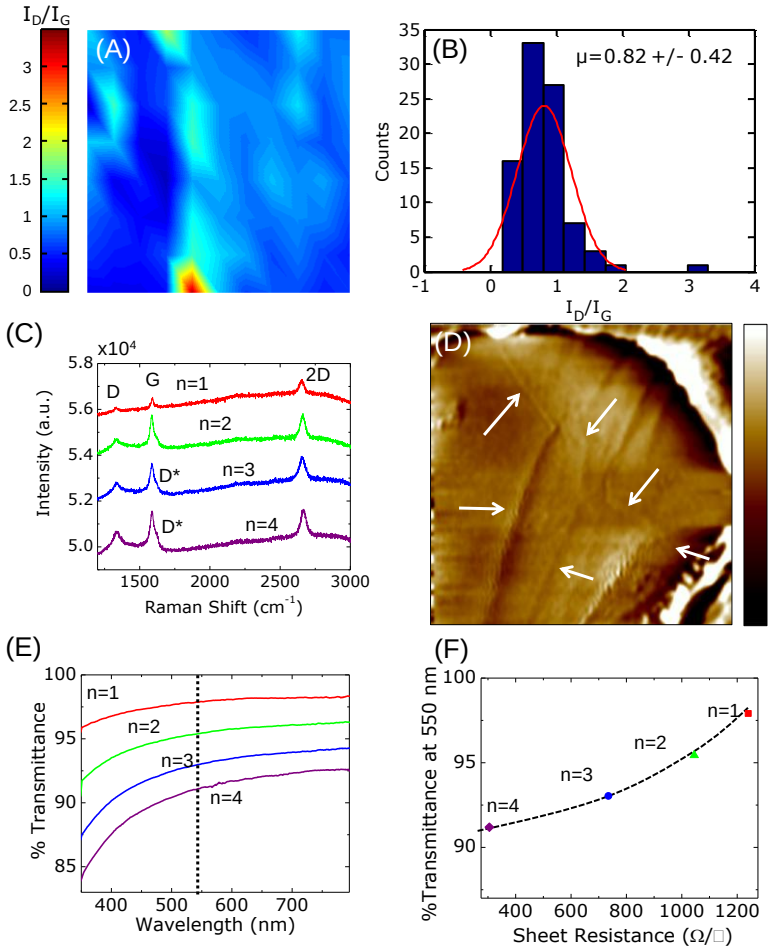

Figure 6.3 Raman and AFM analysis of a CVD graphene. **(A)** Integrated intensity ratio of the D-peak to G-peak (I_D/I_G) used to extract crystallite size (L_a) in Figure 6.2. **(B)** Histogram of data in (A), with mean and standard deviation as indicated. **(C)** Point Raman spectra of LBL assembled graphene layers (n =1 to 4) showing increasing disorder and layer number. **(D)** 1 by 1 μm AFM scan of freely suspended graphene over a 1 μm hole in a TEM grid. The height bar is 1.6 nm, and the arrows indicate the locations of grain boundaries. The graphene domain sizes are on the order of the value obtained by Raman analysis. **(E)** %Transmittance of LBL assembled graphene films from 300 to 800 nm. The dashed line indicates the %Transmittance at 550 nm in (F). **(F)** %Transmittance vs. sheet resistance showing a decrease in both as the thickness of the LBL assembled graphene stacks increases. The dashed line is a guide to the eye.

good agreement with AFM images of our CVD graphene suspended over transmission electron microscopy grids [32] (Figure 6.3 (D)). We note this is not necessarily the distance between graphene grain boundaries, but rather the distance between Raman active linear defects, which may include layer number mismatches, graphene grain boundaries, and graphene wrinkles. Previous scanning tunneling microscopy studies of our CVD graphene revealed the regions between the line defects are almost pristine, i.e. no point defects where detected, with large perturbations

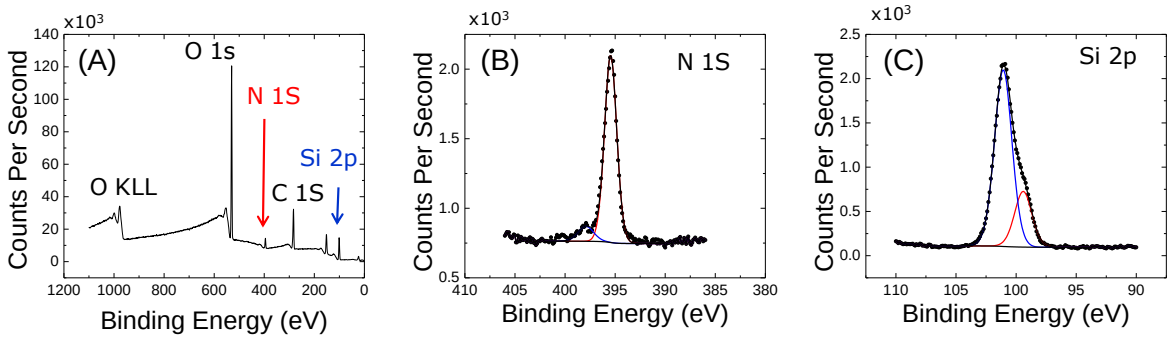

Figure 6.4 XPS analysis of supporting dielectric membrane **(A)** XPS survey. **(B)** N 1S spectra. **(C)** Si 2p spectra. The data indicate the supporting membrane has a $Si_3N_{3.3}$ stoichiometry.

in the material's electronic properties at linear defects [33]. Raman data of LBL assembled graphene stacks show a decreasing I_{2D}/I_G ratio (Figure 6.3 (C)), which is indicative of increasing layer numbers. The data also show an increasing D-peak intensity with increasing transfers. Interestingly, the D*-peak (small shoulder on the G-peak) appears after the third transfer, indicative of increasing sp^3 like character of the graphene defects, or possibly due to increasing PMMA residues within the stack.

Optical absorbance measurements were performed using a Varian CARY 5G system photospectrometer. The sheet resistance of the graphene was measured using a HL5500PC Hall effect measurement system in a Van der Pauw configuration. Atomic force microscope (AFM) data for the substrate and graphene on substrate were collected using a Digital Instruments Dimension 3000 AFM in a tapping mode. Calculated RMS roughness values were obtained using Nanoscope Analysis v.1.4 software from Bruker Corporation after flattening the raw data. XPS is accomplished using a KRATOS Axis Ultra 165 mm X-ray photoelectron spectrometer, and conducted at various locations of our supporting SiN films to elucidate the stoichiometry of the PECVD deposited SiN. XPS of our CVD graphene films has been previously reported (see Chapter 5). Figure 6.4 shows the survey, N 1S, and Si 2p XPS spectra used to calculate the supporting membrane stoichiometry. We find the PECVD SiN results in a $Si_3N_{3.3}$ stoichiometry.

6.4 Measurement Setup, COMSOL Simulation, and Results

The heater and sensor of the device under test (DUT) are wirebonded to a KYOCERA leaded ceramic chip carrier, prior to being placed in a Janis vacuum probe station for measurement. The probe station is capable of reaching vacuum levels down to 10^{-6} torr and has a wide temperature range of 25 to 650 K. We use liquid nitrogen cooling and investigate a smaller temperature range, which captures the majority of the physics for thermal transport in the diffusive regime of our samples. Prior to all measurements the device is annealed for ≈8 hours in vacuum at 450 K to stablize the resistance of all the metal electrodes. The heater and sensor resistances are calibrated as a function of temperature from 80 to 450 K. This is done using a four-point Delta Mode technique and the Keithley 6221/2182A current source and nanovoltmeter combo. Current is applied to the heater using a Keithley 4200-SCS and heater power is monitored with a four-point current-voltage measurement. The resistance of the sensors is monitored by a four-point Delta Mode technique. The ambient temperature is controlled with a Lakeshore model 377 temperature controller. Our measurements are done under vacuum where heat loss due to convection is neglible. The maximum heat loss due to radiation (Q_{rad}) is ≈1% at 400 K, where $Q_{rad} = 4\sigma\epsilon A T_0^3 (T-T_o)$. Here, σ is the Stefan-Boltzman constant, ϵ is the emmissivity (assumed to be 1 to provide an upper bound), A is the area of the suspended membrane, T_o is the background temperature, and T is the temperature of the heater.

Similarly to previous work from our group, we use a commercial software package (COMSOL Multiphysics) to extract the thermal properties of graphene from the electrical thermometry data [67]. Figure 6.5 shows our thermal circuit, the optimized 3-dimensional finite element method (FEM) model of the suspended thermometry platform, and a typical extracted steady-state temperature profile when a graphene film is placed on one side of the platform. The

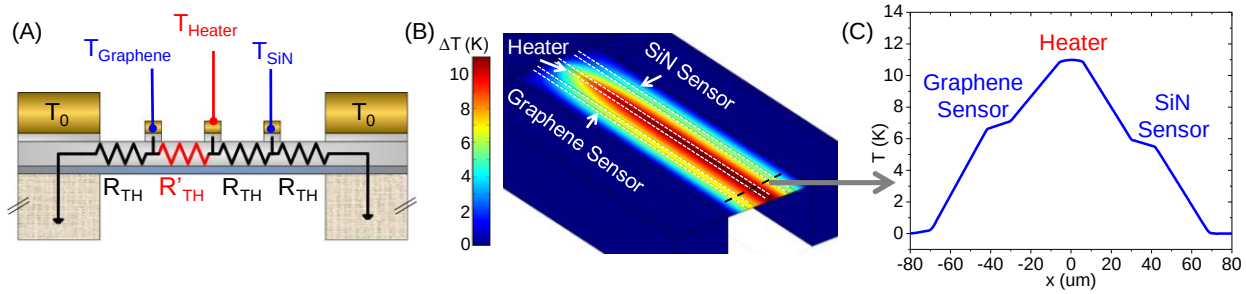

Figure 6.5 (A) Equivalent thermal circuit for our suspended thermometry platform. **(B)** 3-dimensional COMSOL model of suspended thermometry platform. **(C)** Typical steady state extracted temperature profile with graphene on one half of the platform. The difference in the temperature sensors can be attributed to the higher G_{TH} of the graphene side of the platform.

simulation is performed using isothermal boundary conditions at the edges of the suspended membrane (i.e. at the Si heat sink), while the symmetry plane and the surface of the supporting membrane and graphene are given adiabatic boundary conditions. Importantly, the 3-dimensional simulations include thermal contact resistance effects [67]. A constant power density is applied to the center heater electrode to simulate Joule heating, and the structure is allowed to come to steady state. We then compare the simulated temperature rises in the sensors to the measured experimental data, effectively using the G_{TH} of the membrane and graphene as a fitting parameter. Additionally, we find that although our suspended membrane geometry confines heat flow along the width of the membrane (i.e. the direction perpendicular to the heater and sensor electrodes, W ≈ 130 μm), approximately 10% of the power is lost to the Si at the top and bottom edges of the membranes (i.e. the edges at the ends of the heater and sensor electrodes, L ≈ 1 mm).

Figure 6.6 shows scanning electron microcroscopy (SEM) images of the typical devices used in this study, from which we measure the device dimensions in order to build our COMSOL models and calculate thermal conductivity. The thickness of the supporting membranes is measured by ellipsometry and compared to cross-sectional SEM images. Our films vary between ≈150 nm and ≈200 nm depending on the fabrication run. The contrasts of the graphene and the

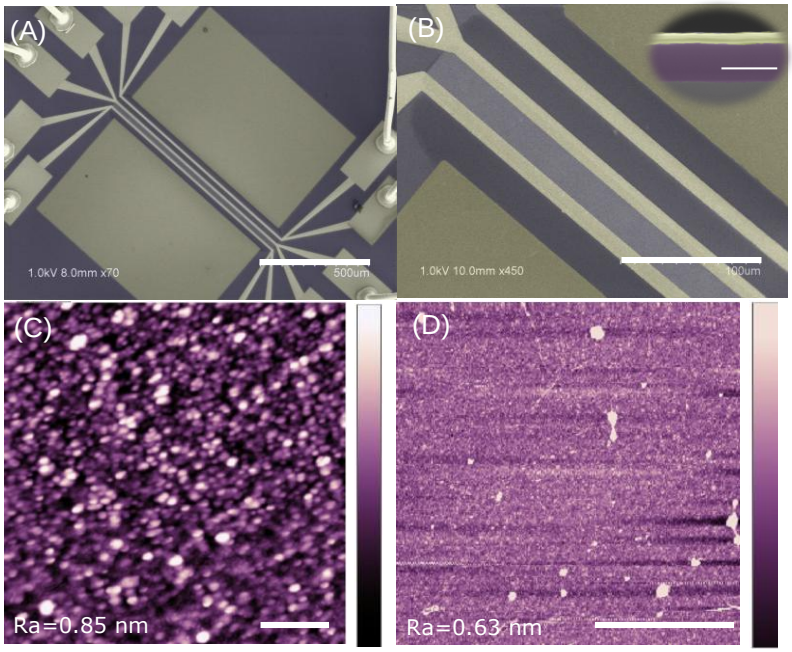

Figure 6.6 (A, B) Scanning electron microscope (SEM) images of suspended thermometry platform with CVD graphene patterned between an edge sensor and the center heater. Scale bars are 500 and 100 μms, respectively. (B-inset) Cross-sectional SEM image of the supporting membrane capped with ≈50 nm of Pd to enhance contrast. Scale bar is 300 nm. **(C, D)** Atomic force microscopy images of PECVD deposited $Si_3N_{3.3}$ without (C) and with (D) transferred CVD graphene. Scale bars are 200 nm and 2 μm, respectively. The height color bar is 6.5 nm.

suspended region of the membrane are easily distinguishble in the final test structure. Atomic force microsopy analysis of the PECVD $Si_3N_{3.3}$ shows our supporting dielectric membranes have an RMS roughness of 0.85 nm (3× higher than SiO_2) with an auto correlation length of ≈80 nm. The RMS roughness decreases slightly after transferring CVD graphene. We note this may vary over different areas of the graphene sheet depending on the cleanliness of the imaged area, i.e. the presence of PMMA residues.

Figure 6.7 (A) shows our measured resistance calibration curves for the heater, graphene sensor, and $Si_3N_{3.3}$ sensor for a sample with a single layer of graphene (n = 1). The measured sensor resistance change ($\Delta R/R_o$) as a function of the power applied to the heater (P) at T = 300 K is shown for both the graphene and $Si_3N_{3.3}$ sample. The difference in slope between the two suggests the side with graphene has a higher G_{TH}. We measure similar R vs. P from 80 to 450 K

for the sensors, as well as for the heater. The slope of these curves (dR/dP) is shown in Figure 6.7 (C). Dividing dR/dP by the inverse of the derivative of our resistance calibration curves (dT/dR) gives us the change in the sensor and heater temperatures with respect to the heater power (dT/dP) (Figure 6.7 (D)). The calculated dT/dP values provide the temperature drop ($\Delta T_G = T_{Heater}-T_{Gsensor}$) across the graphene-$Si_3N_{3.3}$ on one side of the platform, and the ($\Delta T_S = T_{Heater}-T_{SiNsensor}$) across the $Si_3N_{3.3}$ membrane on the other side. The dT/dP values are used as inputs to our COMSOL model to simulate the thermal transport of the platform under and applied heating power as previously described.

The extracted G_{TH} values for our n = 1 sample are shown in Figure 6.8 (A). It is easily seen that the G_{TH} of the graphene-$Si_3N_{3.3}$ side is significantly higher than that of the supporting $Si_3N_{3.3}$

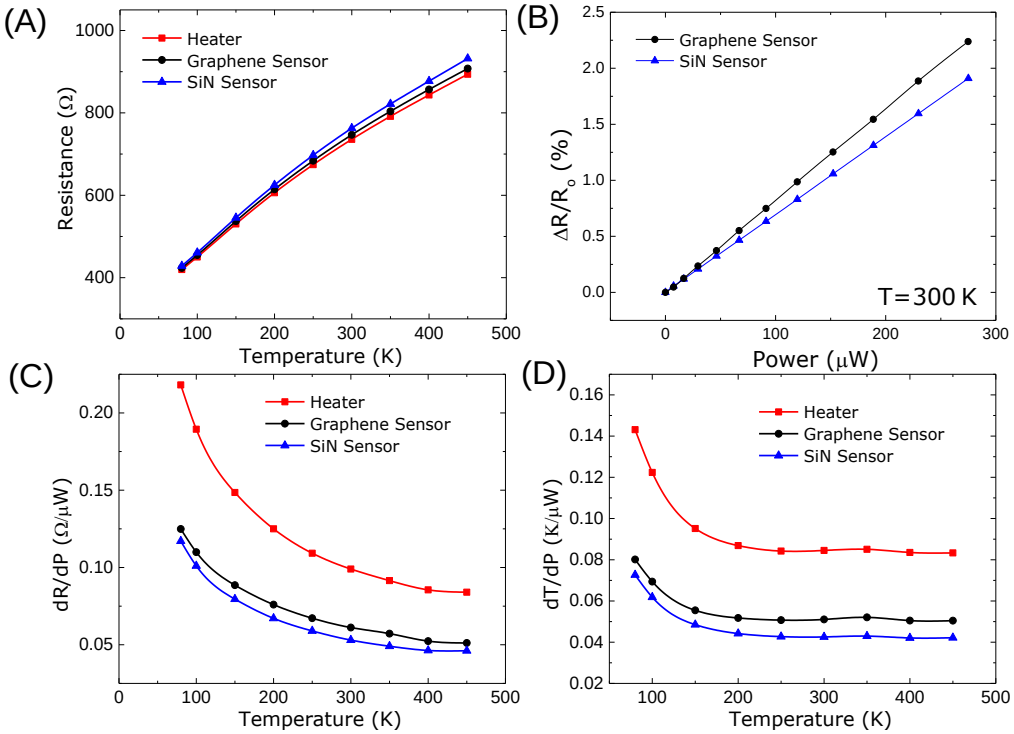

Figure 6.7 (A) Resistance calibration vs. temperature for the heater, graphene sensor, and $Si_3N_{3.3}$ sensor. **(B)** Normalized change in resistance vs. heater power at 300 K for the graphene sensor and the $Si_3N_{3.3}$ sensor. The difference in the slope (dR/dP) is indicative of higher G_{TH} on the graphene side of the platform. **(C)** Measured dR/dP data for the heater and sensors from 80 to 450 K. **(D)** Change in heater and sensor temperatures with respect to heater (dT/dP) power vs. temperature, calculated using the data in (C) and the derivative of the data in (A).

side alone. The addition of the graphene accounts for up to 40% of the total G_{TH} on the graphene side at T = 450 K (Figure 6.8 (A) inset). We do not notice a significant temperature hysteresis in our measurement when performing measurements with increasing and decreasing ambient temperature sweeps. We repeated our measurements on a second sample for n = 1 layers of CVD transferred graphene and found similar results. The extracted thermal conductivity for both samples are shown in Figure 6.8 (B). We note that although our uncertainty (~20 % at 300 K) is better than that of Raman optothermal measurements for substrate supported CVD graphene [55], this is still a rather large error for electrical thermometry. The uncertainty can be improved

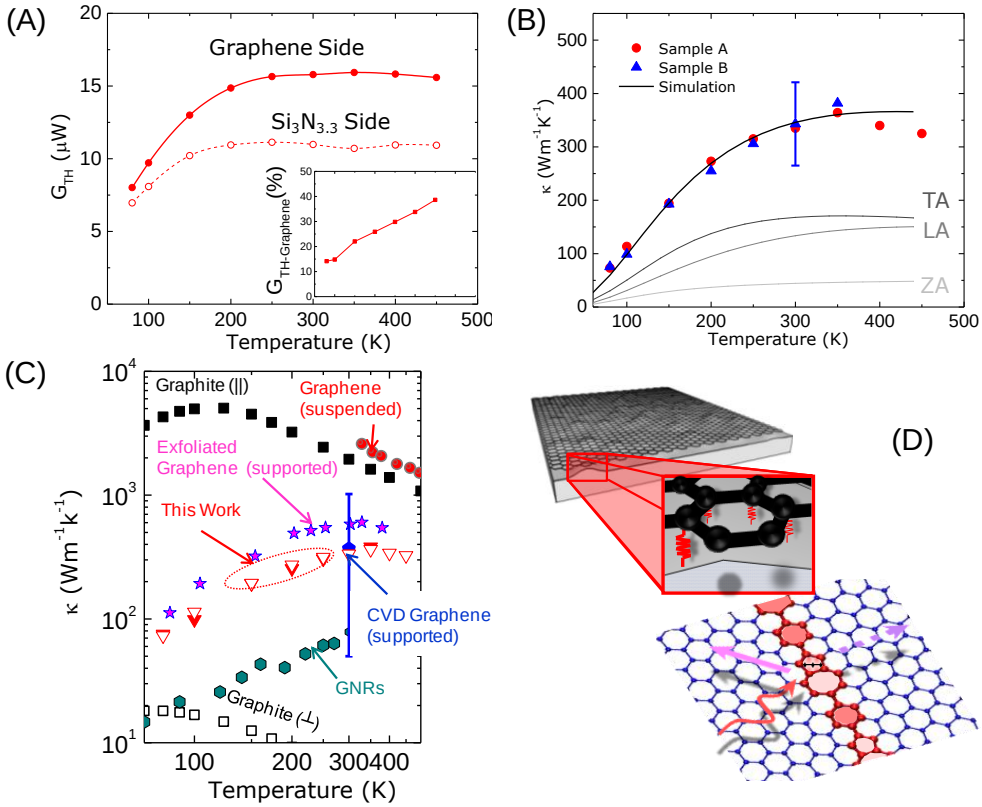

Figure 6.8 (A) Thermal conductance (G_{TH}) vs. temperature for graphene-$Si_3N_{3.3}$ (solid circles) and $Si_3N_{3.3}$ side (open circles) of the thermometry platform for n = 1 layers of CVD graphene. The inset shows the percentage of the thermal conductance attributed to the graphene. **(B)** Extracted thermal conductivity (symbols) compared to NEGF calculations (lines) with a grain size of 80 nm. **(C)** Comparison of our data to reported values for graphene in the literature [3, 47, 52, 55, 67]. **(D)** Schematic representations of CVD graphene coupling to the supporting substrate and phonon scattering (solid magenta arrow) / transmission (dashed magenta arrow) at a graphene grain boundary.

by thinning the supporting membrane to enhance the G_{TH} ratio of the graphene to dielectric membrane. Additionally, a more thorough uncertainity analysis across the full temperature range is still being performed.

6.5 Discussion and Conclusions

We compare our extracted thermal conductivity to NEGF calculations (Figure 6.8 (B)) to elucidate the role of substrate phonon and grain boundary scattering (Figure 6.8 (D)) on thermal transport in substrate supported CVD graphene. Details of the model are reported in [38]. The thermal conductivity is the sum of the individual transverse (TA), longitudinal (LA), and flexural acoustic (ZA) phonon modes. The best fit to the experimental data is obtained using a grain size (L_g) of 80 nm, which is in fairly good agreement with the crystallite size extracted by Raman spectroscopy (Figure 6.2 (C)). We note the model is calibrated for exfoliated graphene on SiO_2, which has a lower surface roughness and slightly larger auto correlation length (≈2×) between asperities, which may account the slight disparity between the Raman active L_a and calculated L_g.

We now turn our attention to the tunable thermal conductivity of LBL assembled graphene vdW solids. Using the fabrication methods and the electrical thermometry techniques described above, we investigated the thermal transport in artificial stacks of n = 1 to n = 4 transferred layers of CVD grown polycrystalline graphene. We note that as the layer numbers increased, lithography become increasingly difficult because the adhesion of the SiO_2 insulating layer and the metal electrodes become exceedingly worse, such that the electrodes would not adhere to the surface of n = 2 to n = 4 layers of graphene. Therefore, we performed an O_2 plasma etch to remove the graphene underneath the electrodes prior to SiO_2 and metal deposition. While this may increase the thermal contact resistance per unit area, we note our thermal contact area is very large

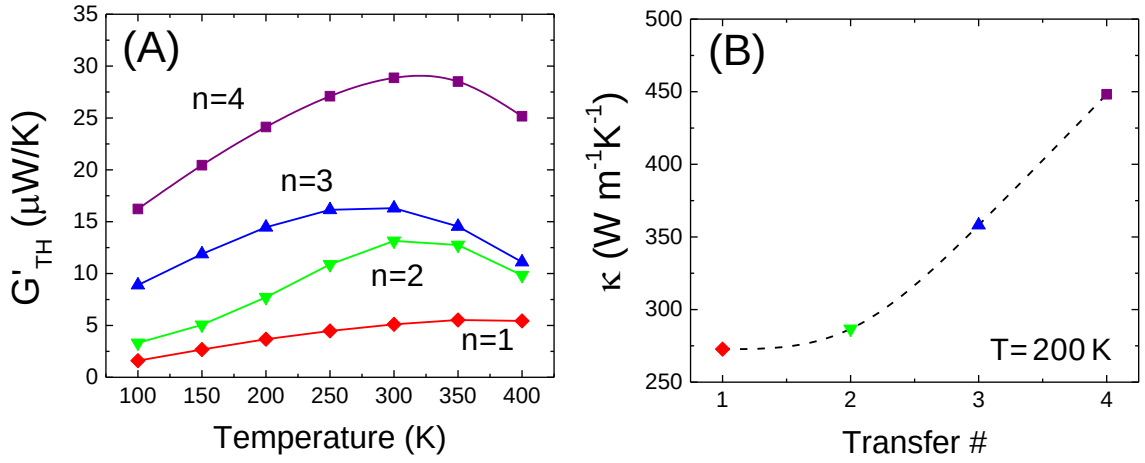

Figure 6.9 (A) Effective thermal conductance (G'_{TH}) of LBL assembled graphene vdW solids vs. temperature for n=1 to 4. The thermal conductance of the substrate has been subtracted and the data have been normalized the minimum sample length and cross section area of the overall graphene-$Si_3N_{3.3}$ stack. **(B)** Calculated κ of LBL assembled graphene vdW solids at T= 200 K for n=1 to 4. The rapid increase after the second transfer suggests a characteristic length scale for substrate phonon scattering.

(≈5000 μm^2 per electrode) and the overall temperature drop at the contacts is negligible, as confirmed by our COMSOL simulations. Figure 6.9 compares the thermal properties of the LBL assembled graphene stacks, normalized to account for differences in dimensions. The normalized thermal conductance (G'_{TH}) of the graphene stacks increases with increasing transfer number as expected. Figure 6.9 (B) compares the thermal conductivity at 200 K for the LBL graphene films. Here, κ is calculated using a simple 1-dimensional heat flow approximation, i.e. $\kappa = G'_{TH} \times L_{sample} / (W_{sample} \times t_{stack})$, assuming the thickness of stack is simply the number of transfers times the thickness of graphene, 3.4 Å. The thermal conductivity increases rapidly after the second layer, suggesting the substrate scattering of LBL vdW solid phonons has a characteristic length on the order of 1 to 2 nm, in agreement with previous studies on mechanically exfoliated graphene [53, 56]. The maximum thermal conductivity reached after four transfers, however, is still significantly lower than the $\kappa||$ of pyrolytic graphite, suggesting thermal transport in our

graphene LBL assemble vdW solids is limited by process induced variables, e.g. polymer residues and graphene wrinkles, as well as the quality and crystallinity of the starting material.

In conclusion, we investigated heat flow in $Si_3N_{3.3}$ supported polycrystalline graphene and graphene based vdW solids. The thermal conductivity of substrate supported CVD graphene is found to be about 2× lower than substrate supported mechanically exfoliated graphene. Comparison to NEGF calculations shows the additional reduction in thermal conductivity is likely due to grain boundary scattering of the LA, TA, and ZA phonon modes of graphene. The thermal conductance and conductivity of graphene based vdW solids is found to increase with increasing layer numbers. This has important technilogical implications for graphene based thermal heat spreaders and emerging vdW solid devices. To our knowledge these results demonstrate the first pratical tuning of thermal transport in a atomic layer-by layer assembled solid provide a powerful means to tune heat flow through the use of 2-dimensional crystals in nanosale interconnects or devices.

6.6 References

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CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

We have described several applied and fundamental properties of carbon nanomaterials and nanoscale devices. We introduced a pulsed measurement method to eliminate unwanted hysteresis of carbon nanotube (CNT) transistors under various conditions, and show that our method results in the extraction of more consistent mobility and threshold voltage values for these devices. We have also directly imaged power dissipation in CNT network transistors using infrared microscopy. By correlating the temperature profile of the device near breakdown conditions we show how the reliability of such devices is limited by the high thermal resistance ($\approx 4.4 \times 10^{11}$ K/W) at crossed CNT junctions.

We then turn our attention from 1-dimensional CNTs to 2-dimensional graphene and investigate the fundamental chemical sensing and thermal transport properties of polycrystalline graphene grown by chemical vapor deposition. We find that 1-dimensional defects are needed to enhance the chemical sensitivity of 2-dimensional materials such as graphene. In addition, confinement of current flow through 1-dimensional defects provides a route towards engineering the chemical sensitivity of graphene. We also report the first electrical thermometry measurements of substrate supported polycrystalline graphene. We find the thermal conductivity at room temperature (≈ 350 $Wm^{-1}K^{-1}$) is significantly lower than substrate supported single crystal graphene obtained by mechanical exfoliation. Additionally, we show how layer-by-layer assembly of polycrystalline graphene vdW solids can lead the tunable thermal

conductivity of ultra-thin graphitic films. The thermal conductivity of up to four layers of stacked CVD graphene is shown to be ≈1.5× that of copper, which has important technological implications for applications such as thermal heat spreaders.

The work presented here has resulted in new knowledge about the reliability and fundamental properties of low-dimensional materials coupled to their 3-dimensional environment. Applying this knowledge to the design of new nanoscale devices and nanomaterials based composites provides a route towards the "bottom-up" design of more energy efficient systems and energy harvesting materials, which could lead to significant reductions in energy consumption by residential and commercial buildings as well as power dissipation in future nanoscale electronics.

7.2 Future Work

It is a widely held belief that nanotechnology will enable our society to tackle many of the daunting grand challenges that it faces, particularly those related to the increasing energy demands and rising healthcare costs of our country and our global society. Carbon nanomaterials, in particular, are poised to have a significant impact in addressing these issues due to their ease of fabrication, and the abundance of carbon on earth with respect to other elements.

The work presented here has already catalyzed collaborations with research groups around the United States and across the globe to further understand the role of crossed CNT junctions on the design and optimization of carbon based macro electronics. Such devices could find applications in flexible and wearable biosensors to monitor biological signals for early disease detection and monitoring progression and prognosis of medical treatments. Such wearable biomedical devices may be limited by weak vdW

coupling of nanomaterials to the supporting substrate, as well as the low thermal conductivity of most polymers. Therefore, further work on understanding and tuning thermal transport and power dissipation of nanomaterials in contact with flexible polymers is needed to develop the design space for such devices.

While the role of crossed CNT junctions on the reliability of CNT network devices has been elucidated, it would be interesting to exploit the fundamental properties of such 0-dimensional systems in the design of nanocomposite materials for energy harvesting (e.g. thermoelectric devices). This application would require a deeper understanding of tuning nanoscale energy transport across the 0-dimensional junctions of 1-dimensional materials.

Finally, the (re)emergence of 2-dimensional transition metal dichalcogenides (TMDCs, e.g. MoS_2 and WS_2) has opened up a variety of new device applications. The original techniques presented in this body of work could be applied to this new class of nanomaterials to further explore the fundamental properties of 2-dimensional TMDCs in contact with their surrounding 3-dimensional environment.